2U Server System

Service Manual

P47

P/N: 2017-MNU-000016
June, 2018 (Revision A)

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Warning!

Before opening the chassis cover, remove all power cords to completely disconnect power from the system.

Contents

About This Manual i

Conventions i
Safety Symbols ii
Safety Precautions iii
Operation Safety iii
Electrical Safety iv
Battery Replacement Safety iv
Laser Peripherals or Devices Safety v
Intended Application Uses v
Site Selection vi
Tools Required vi
Regulatory and Integration Information vii
Regulatory Compliance Identification Numbers vii
Product Regulatory Compliance vii
Power Cords ix
Rack Mount Instructions x

1 Introduction 1-1

1.1 Audience Assumptions 1-1
1.2 Manual Organization 1-1
1.3 Packing Checklist 1-1
1.4 Specifications 1-2
1.5 Product Features 1-2
1.6 System Overview 1-4
1.6.1 Server Chassis Layout 1-4
1.6.2 Motherboard Layout 1-6
1.6.3 Front View 1-8
1.6.4 Back View 1-9
1.6.5 Buttons and System LED Information 1-9
1.6.6 System Thermal Solution 1-12

2 Hardware Operations 2-1

2.1 Before You Start 2-1
2.1.1 Power Off 2-1
2.2 Rear Chassis Cover 2-2
2.2.1 To remove the rear chassis cover 2-2
2.2.2 To install the rear chassis cover 2-3
2.3 Front Top Cover 2-5
2.3.1 To remove the front top cover 2-5
2.3.2 To install the front top cover 2-6
2.4 Cable Guide 2-6
2.4.1 To remove the cable guide 2-7
2.4.2 To install the cable guide 2-7
2.5 Stiffener 2-8
2.5.1 To remove the stiffener 2-8
2.5.2 To install the stiffener 2-9
2.6 Motherboard 2-9
2.6.1 To remove the motherboard 2-10
2.6.2 To install the motherboard 2-10
2.7 Processor 2-11
2.7.1 To remove the heat sink 2-12
2.7.2 To install the heat sink 2-12
2.7.3 To remove the processor 2-13
2.7.4 To install the processor 2-14

2.8 System Memory 2-15
2.8.1 To remove the system memory 2-17
2.8.2 To install the system memory 2-17
2.9 Power Supplies 2-18
2.9.1 To remove the power supply 2-19
2.9.2 To install the power supply 2-19
2.10 System Fans 2-20
2.10.1 To remove the system fans 2-21
2.10.2 To install the system fans 2-21
2.11 2.5” HDDs 2-22
2.11.1 To remove the 2.5” HDD 2-22
2.11.2 To install the 2.5” HDD 2-23
2.12 8x2.5” HDDs Backplane 2-24
2.12.1 To remove the 8x2.5” HDDs backplane 2-25
2.12.2 To install the 8x2.5” HDDs backplane 2-25
2.13 Front Panels 2-26
2.13.1 To remove the front panel 2-27
2.13.2 To install the front panel 2-27
2.14 OCP Card (Optional) 2-28
2.14.1 To remove the OCP card 2-28
2.14.2 To install the OCP card 2-29
2.15 Expansion Cards 2-29
2.15.1 To remove the expansion card 2-30
2.15.2 To install the expansion card 2-31
2.16 Fan Duct 2-32
2.16.1 To remove the fan duct 2-32
2.16.2 To install the fan duct 2-33

3 Connectors 3-1

3.1 Backplane Connectors 3-1
3.2 OCP Card Connectors 3-2

4 Cable Routing 4-1

Appendix 1 Hazardous Substances Free Regulations and Electromagnetic Emissions Notices I

China RoHS Regulations I
Taiwan BSMI II
Electromagnetic Emissions Notices III
Federal Communications Commission notice III
Notices for Canada (Avis Canadien) III
Notices for China III
Notices for European Union IV
Notices for Japan IV
Notices for Korea IV
Notices for Taiwan V
Notices for Russia V

Appendix 2 BIOS SPEC

Appendix 3 BMC SPEC

About This Manual

Conventions
Safety Symbols
Safety Precautions
Regulatory and Integration Information
Rack Mount Instructions

About This Manual

Conventions

To make sure that you perform certain tasks properly, take note of the following symbols used throughout this manual.

	**Warning:**	Information to prevent injury to yourself when trying to complete a task.
	**Caution:**	Information to prevent damage to the components when trying to complete a task.
	**Important:**	Information that you must follow to complete a task.
	**Note:**	Tips and information to aid in completing a task.

Safety Symbols

Before troubleshooting, you must be familiar with the safety information listed below. In order to avoid any potential hazards, the following symbols may be placed on some components of the server.
The shape and the color of symbols shown below are mainly for your reference. Please take the actual shipment as standard.

	Indicates the potential hazard of energy circuits or electric shock. To reduce the risk of injury from electric hazards, do not open this enclosure. **Warning:** Any surface or area of the equipment marked with this symbol indicates the presence of electric shock hazards. The enclosed area contains no operator serviceable parts.
	Indicates the potential hazard of electric shock. The enclosed area contains no user of field serviceable parts. Do not open for any reason. **Warning:** To reduce the risk of injury from electric shock hazards, do not open this enclosure.
	Indicates the presence of a hot surface or hot component. **Warning:** To reduce the risk of injury from a hot component, allow the surface to cool before touching it.
	Any RJ45 receptacle marked with this symbol indicates a network interface connection. **Warning:** To reduce the risk of electric shock, fire, or damage to the equipment, do not plug telephone or telecommunications connectors into this receptacle.
	This symbol, on power supplies or systems, indicates that the equipment is supplied by multiple sources of power. **Warning:** To reduce the risk of injury from electric shock, remove all power cords to completely disconnect power from the system.
 Weight in kg. Weight in lb.	This symbol indicates that the component exceeds the recommended weight for one individual to handle safely. **Warning:** To reduce the risk of personal injury or damage to the equipment, observe local occupational health and safety requirements and guidelines for manual material handling.

Safety Precautions

Observe the following safety precautions when you are connecting or disconnecting any device.

- Regarding the standards of workstation regulations, do not place the server in the visual field of the user, because of the glossy front of the case.
- The product is non-consumer product and for profession technical person used only.

Operation Safety

- Any operation on this server must be conducted by certified or experienced engineers.
- Before operating your server, carefully read all the manuals included with the server package.
- Before using the server, make sure that all cables are correctly connected and power cords are not damaged. If any damage is detected, contact your dealer as soon as possible.
- To avoid short circuits, keep paper clips, screws, and staples away from connectors, slots, sockets and circuitry.
- Before opening the chassis panels, make sure all power cords are unplugged.
- Avoid dust, humidity, and extreme temperatures; place the server on a stable surface.
- If the power supply is broken, do not try to fix it by yourself. Contact an authorized dealer.
- It is recommended that you wear gloves when assembling or disassembling the server to protect from cuts and scrapes.
- When the server is powered on, heat sinks and the surfaces of certain IC devices may be hot. Do not touch them. Check whether the fans are functioning properly.

Electrical Safety

- Before installing or removing signal cables, ensure that the power cords for the system unit and all attached devices are unplugged.
- To prevent electric shock hazard, disconnect the power cable from the electrical outlet before relocating the system.
- When adding or removing any additional device to or from the system, ensure that the power cords for those devices are unplugged before the signal cables are connected. If possible, disconnect all power cords from the existing system before you add a device.
- Use one hand, when possible, to connect or disconnect signal cables to prevent a possible shock from touching two surfaces with different electrical potentials.

- This product is equipped with a three-wire power cable and plug for user safety. Use the power cable with a properly grounded electrical outlet to avoid electric shock.

Motherboards, adapters, and disk drives are sensitive to static electricity discharge. These devices are wrapped in antistatic bags to prevent this damage. Take the following precautions:

- If you have an antistatic wrist strap available, use it while handling the device.
- Do not remove the device from the antistatic bag until you are ready to install the device in the system unit.
- With the device still in its antistatic bag, touch it to a metal frame of the system.
- Grasp cards and boards by the edges. Hold drives by the frame. Avoid touching the solder joints or pins.
- If you need to lay the device down while it is out of the antistatic bag, lay it on the antistatic bag. Before picking it up again, touch the antistatic bag and the metal frame of the system unit at the same time.
- Handle the devices carefully to prevent permanent damage.

Battery Replacement Safety

This server is provided with an internal Lithium battery or battery pack. There is a danger of explosion and risk of personal injury if the battery is incorrectly replaced or mistreated.
For more information about battery replacement or proper disposal, contact an authorized reseller or your authorized service provider.

This server contains an internal Lithium Manganese Dioxide, or a Vanadium Pentoxide, or an alkaline battery pack. There is risk of fire and burns if the battery pack is not handled properly. To reduce the risk of personal injury:

- Do not attempt to recharge the battery.
- Do not expose to temperatures higher than 70°C.
- Do not disassemble, crush, puncture, shorten external contacts, or dispose in fire or water.
- Replace only with the spare parts designated for this product.

Batteries should not be littered along with the general household waste. Please use the public collection system or return them to the supplier.

Laser Peripherals or Devices Safety

To avoid risk of radiation exposure and/or personal injury:

- Do not open the enclosure of any laser peripheral or device.
- Laser peripherals or devices are not user serviceable.
- Return to manufacturer for servicing.

Intended Application Uses

This product was evaluated as Information Technology Equipment (ITE), which may be installed in server rooms, computer rooms and similar commercial type locations. The suitability of this product for other product categories and environments (such as medical, industrial, residential, alarm systems, and test equipment), other than an ITE application, may require further evaluation.

Site Selection

Restricted Access Location: location for equipment is intended for installation only in a Server Room or Computer Room where both of the following apply:

- Access can only be gained by SERVICE PERSONS about the reasons for the restrictions applied to the location and about any precautions that shall be taken.
- Access is through the use of a TOOL or lock and key, or other means of securtiy, and is controlled by the authority responsible for the location.

The system is designed to operate in a typical office environment. Choose a site that is:

- Clean, dry, and free of airborne particles (other than normal room dust).
- Well-ventilated and away from sources of heat including direct sunlight and radiators.
- Away from sources of vibration or physical shock.
- Isolated from strong electromagnetic fields produced by electrical devices.
- In regions that are susceptible to electrical storms, we recommend you plug your system into a surge suppresser and disconnect telecommunication lines to your modem during an electrical storm.
- Provided with a properly grounded wall outlet.
- Provided with sufficient space to access the power supply cord(s), because they serve as the product's main power.
- Mechanical Loading – Mounting of the equipment in the rack should be such that a hazardous condition is not achieved due to uneven mechanical loading.

Tools Required

A cross screwdriver or a flat screwdriver is needed to install or remove the components in the server.

Regulatory and Integration Information

Regulatory Compliance Identification Numbers

For the purpose of regulatory compliance certifications and identification, this server is assigned a serial number. This server serial number can be found on the product label, along with the required approval markings and information. When requesting certification information for this product, always refer to this serial number. This serial number should not be confused with the marketing name or model number.

Product Regulatory Compliance

Worldwide Safety approvals can be supplied according to the requirements from Marketing or Customer.

Product Safety Compliance

The designs of server complies with the following safety requirements:

Table i Product Safety Requirements

IEC 60950-1	Safety of Information Technology Equipment
EN 60950-1	Safety of Information Technology Equipment Including Electrical Business Equipment, European Committee for Electrotechnical Standardization (CENELEC)
UL 60950-1	Safety of Information Technology Equipment
UL 94	Tests for Flammability of Plastic Materials for Parts in Devices & Appliances
GB4943	Safety of Information Technology Equipment

Product EMC Compliance

This product has been tested and verified to comply with the following electromagnetic compatibility (EMC) regulations.

Communications Commission Notice

Part 15 of the Federal Communications Commission (FCC) Rules and Regulations has established Radio Frequency (RF) emission limits to provide an interference-free radio frequency spectrum. Many electronic devices, including computers, generate RF energy incidental to their intended function and are, therefore, covered by these rules. These rules place computers and related peripheral devices into two classes, A and B, depending upon their intended installation. Class A devices are those that may reasonably be expected to be

installed in a business or commercial environment. Class B devices are those that may reasonably be expected to be installed in a residential environment (for example, personal computers). The FCC requires devices in both classes to bear a label indicating the interference potential of the device, as well as additional operating instructions for the user.
The rating label on the device shows which class (A or B) the equipment falls into. Class A devices do not have an FCC logo or FCC ID on the label. Class B devices have an FCC logo or FCC ID on the label. Once the class of the device is determined, refer to the following corresponding statement.

Class A Equipment

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at personal expense.

Declaration of Conformity for Products Marked with the FCC Logo—United States Only

This device complies with Part 15 of the FCC Rules Operation and is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
For questions regarding your product, please contact the supplier.
To identify this product, refer to the Part, Series, or Model number found on the product.

European Union Notice

Products with the CE Marking comply with both the EMC Directive (89/336/EEC) and the Low-Voltage Directive (73/23/EEC) issued by the Commission of the European Community.
Compliance with these directives implies conformity to the following European Norms (in brackets are the equivalent international standards):

Table ii European Union EMC Requirements

EN55032 (CISPR 32)	Electromagnetic Interference
EN55024 (IEC61000-4-2,3,4,5,6,8,11)	Electromagnetic Immunity
EN61000-3-2 (IEC61000-3-2)	Power Line Harmonics
EN61000-3-3 (IEC61000-3-3)	Power Line Flicker

Canadian Notice (Avis Canadien)

Class A Equipment

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Japanese Notice

VCCIマークが付いていない場合には、次の点にご注意下さい。

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Taiwanese Notice

警告使用者：

這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策。

Power Cords

The power cord set included in the server meets the requirements for use in the country where the server was purchased. If this server is to be used in another country, purchase a power cord that is approved for use in that country.

The power cord must be rated for the product and for the voltage and current marked on the product's electrical ratings label. The voltage and current rating of the cord should be greater than the voltage and current rating marked on the product. In addition, the cross-sectional area of the wires must be a minimum of 1.00mm² or 18AWG, and the length of the cords must be between 1.8m (6 feet) and 3.6m (12 feet). If you have questions about the type of power cord to use, contact an authorized service provider.

Route power cords so that they will not be walked on or pinched by items placed upon or against them. Pay particular attention to the plug, electrical outlet, and the point where the cords exit from the product.

Rack Mount Instructions

The following or similar rack-mount instructions are included with the installation instructions:

- Elevated Operating Ambient - If installed in a closed or multi-unit rack assembly, the operating ambient temperature of the rack environment may be greater than room ambient. Therefore, consideration should be given to installing the equipment in an environment compatible with the maximum ambient temperature (Tma) specified by the manufacturer.
- Reduced Air Flow - Installation of the equipment in a rack should be such that the amount of air flow required for safe operation of the equipment is not compromised.
- Mechanical Loading - Mounting of the equipment in the rack should be such that a hazardous condition is not achieved due to uneven mechanical loading.
- Circuit Overloading - Consideration should be given to the connection of the equipment to the supply circuit and the effect that overloading of the circuits might have on overcurrent protection and supply wiring. Appropriate consideration of equipment nameplate ratings should be used when addressing this concern.
- Reliable Earthing - Reliable earthing of rack-mounted equipment should be maintained. Particular attention should be given to supply connections other than direct connections to the branch circuit (e.g. use of power strips).

Chapter 1
Introduction

Audience Assumptions
Manual Organization
Packing Checklist
Specifications
Product Features
System Overview

1 Introduction

1.1 Audience Assumptions

This document is for the person who installs, administers, and troubleshoots servers and storage systems. Inventec assumes you are qualified in the servicing of computer equipment and trained in recognizing hazards in products with hazardous energy levels.

1.2 Manual Organization

This manual introduces the chassis along with the hardware information, and how to replace the hardware and connect the cables. This manual is generally organized as follows:

Table 1-1 Manual Introduction

Introduction	General server introduction.
Hardware Operations	The operation of the components on the chassis, such as power supply, power distribution board, system fans, backplane, and riser card.
Connectors	Information about connectors on the various boards in the system.
Cable Connections	How to connect cables correctly.
Appendix	China RoHS Regulations information.

1.3 Packing Checklist

Make sure you have all the components shipped with your system. If any item contained in the package is damaged or missing, please contact your local dealer for replacement. In addition, keep the box and packing materials for possible future use. The server is shipped with the following:

Table 1-2 Packing Checklist

Chassis	➢ 2U rack-mounted chassis
Cables	➢ Main power cable, backplane power cable, SATA/SAS HDD cable, system fan cables, front panel cables, and so forth

1.4 Specifications

The table below is the technical specifications for the server.

Table 1-3 Specifications

Dimensions	➢ Height: 8.69cm ➢ Width: 43.69cm ➢ Length: 73.66cm
Weight	➢ Max. Weight: 24.96KG
Temperature	➢ Operating System: +5°C ~ +35°C ➢ Non-operating System: -40°C ~ +70°C
Humidity	➢ Operating System: +20% ~ +80% ➢ Non-operating System: +10% ~ +90%
Voltage	➢ 100-240VAC input, 1600Watt (1 power supply) ➢ 100-240VAC input, 3200Watt (2 power supplies)
Current	➢ 10-4A (1 power supply) ➢ 20-8A (2 power supplies)

1.5 Product Features

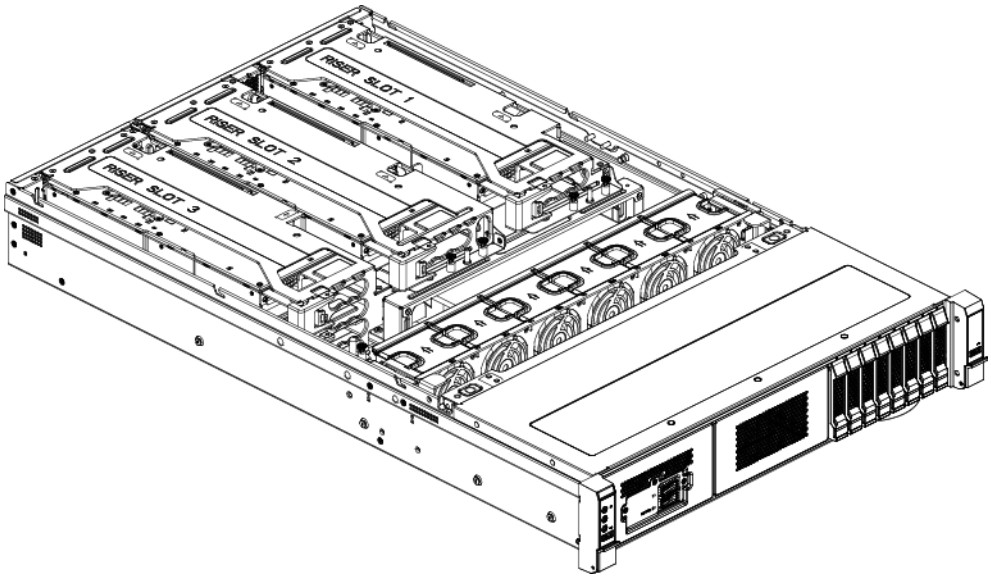


Figure 1-1 Product Introduction with OCP Card

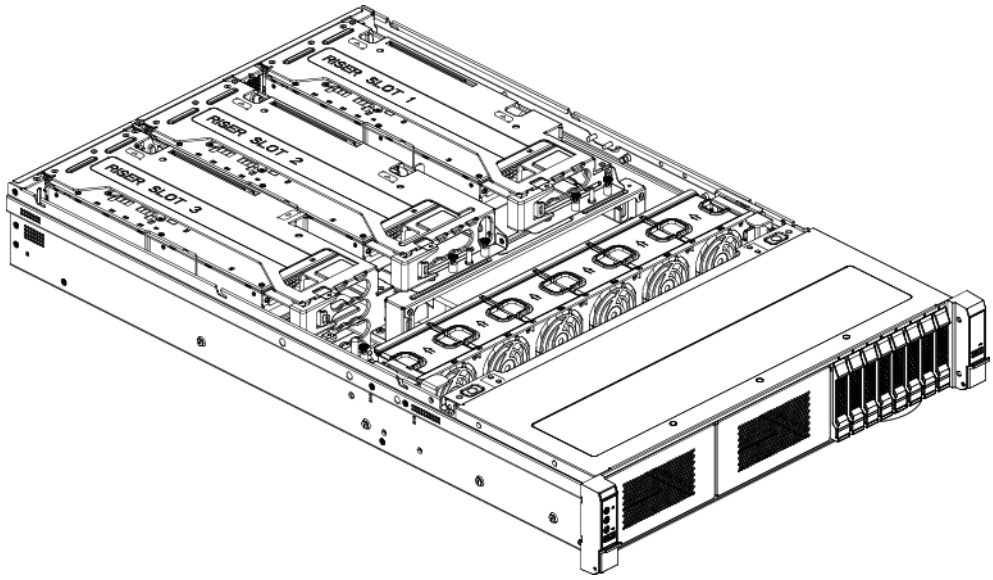


Figure 1-2 Product Introduction without OCP Card

Table 1-4 Product Features

Chassis	➢ 2U rack-mounted chassis
Power	➢ 1x 1600W/2000W Platinum power supply ➢ Or 2x1600W/2000W redundant Platinum power supplies
Storage	➢ 8x2.5” hot-pluggable HDDs
Backplane	➢ 8x2.5” HDD Passive Backplanes
System Fan	➢ Number of fan cage: 6
Processor	➢ 1x AMD Naples SP3 processor ➢ Up to 150W ~ 200W thermal design power (TDP) ➢ Up to 4 Die 8 core per Die ➢ Up to 8 16-bit IO links
System Memory	➢ 16x DDR4 DIMM slots ➢ 8 channels per processor ➢ Supports ECC registered DIMM(RDIMM) at 1866/2133/2400/2667MHz
BMC	➢ Aspeed AST2500 BMC
Onboard Storage Ports	➢ Up to 8x SATA 6Gb/s ports ➢ 2x M.2 NVMe Connecors ➢ 2x U.2 NVMe Connecors
Rear IO Ports	➢ 1x USB Port 3.0 ➢ 1x VGA Port ➢ 1x management Port ➢ 1x Serial Port

Onboard Slots	➢	3xPCI-E x16 Gen3 slots

1.6 System Overview

1.6.1 Server Chassis Layout

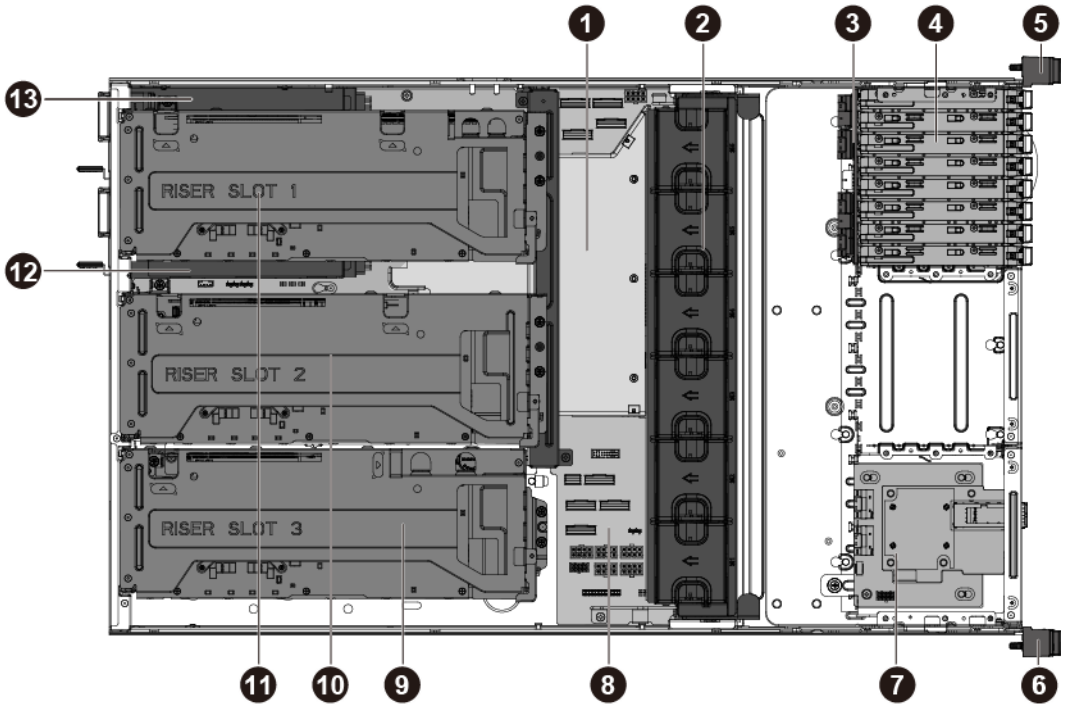


Figure 1-3 System Overview with OCP Card

1	Fan Duct
2	System Fans
3	2.5” HDD Backplane
4	2.5” HDD Bays
5	Front Panel 2
6	Front Panel 1
7	OCP Card (Optional)
8	Motherboard
9	Expansion Card Assembly of GPU 3&4
10	Expansion Card Assembly of GPU 2
11	Expansion Card Assembly of GPU 1
12	Power Supply 1
13	Power Supply 2

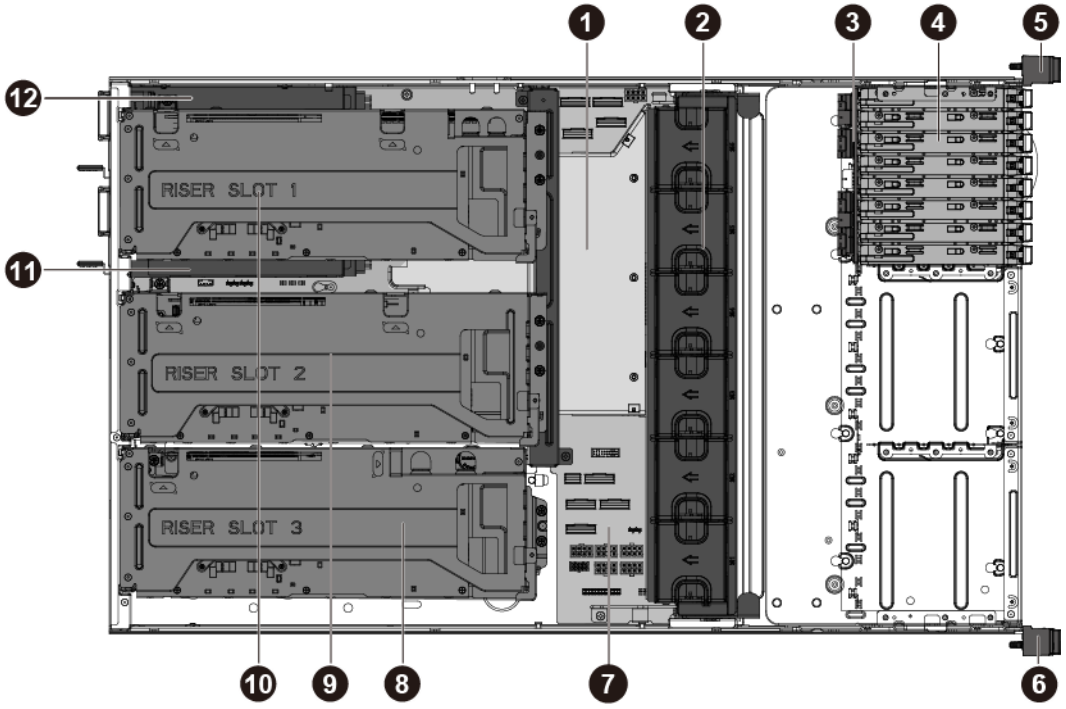


Figure 1-4 System Overview without OCP Card

1	Fan Duct
2	System Fans
3	2.5” HDD Backplane
4	2.5” HDD Bays
5	Front Panel 2
6	Front Panel 1
7	Motherboard
8	Expansion Card Assembly of GPU 3&4
9	Expansion Card Assembly of GPU 2
10	Expansion Card Assembly of GPU 1
11	Power Supply 1
12	Power Supply 2

1.6.2 Motherboard Layout

The layout of the motherboard is shown below. Each connector and major components are identified by number.

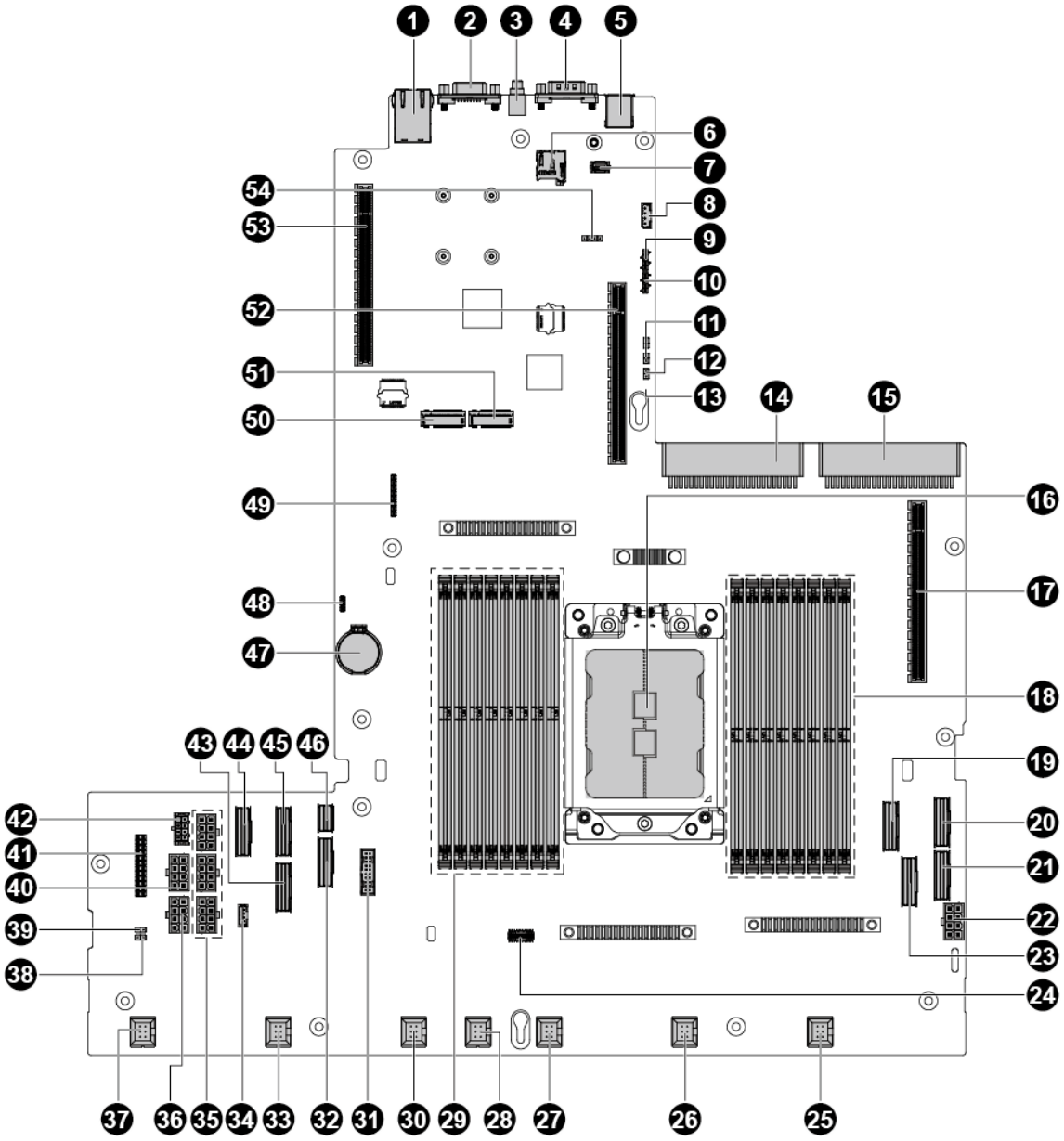


Figure 1-5 Connectors and Component Locations of Motherboard

1	Management Port (J34)
2	VGA Connector (J35)
3	UID Button (SW2)
4	Serial Port (J67)
5	Rear Single USB Port (J33)

6	Micro-SD Card Socket (J50)
7	TPM Connector (J58)
8	IPMB Connector (J36)
9	BMC SIO connector (J66)
10	CPU UART 1x4 connector (J45)
11	BMC Intruder Jumper (J68)
12	BIOS Recovery Jumper (J75)
13	Password Clear Jumper (J76)
14	Power Supply Connector (J1)
15	Power Supply Connector (J73)
16	Processor
17	PCI-E X16 Gen3 Slot1 (J21)
18	DIMM Slots (J10, J11, J12, J13, J14, J15, J16, J17)
19	PCI-E x8 Slimline Connector (G3) (J46)
20	PCI-E x8 Slimline Connector (G2) (J19)
21	PCI-E x8 Slimline Connector (G3) (J20)
22	HDD Backplane Power Connector (J53)
23	SATA Slimline Connector Port 1 (G2) (J71)
24	AMD HDT connector (J47)
25	Fan Connector 1 (J37)
26	Fan Connector 2 (J38)
27	Fan Connector 3 (J39)
28	Fan Connector 7 (J98)
29	DIMM Slots (J3, J61, J5, J60, J6, J7, J8, J9)
30	Fan Connector 4 (J40)
31	Front Panel USB Connector (J57)
32	PCI-E x8 Slimline Connector (G1) (J24)
33	Fan Connector 5 (J41)
34	3.5” HDD Backplane I^2C Signals Connector (J101)
35	GPU Power Connectors (J18, J23, J78)
36	HDD Backplane +5V Power Connector (J100)
37	Fan Connector 6 (J42)
38	System Reset Jumper (J65)
39	NMI Jumper (J70)
40	GPU Power Connector (J77)
41	Front Panel Connector (J48)

42	OCP Power Connector (J99)
43	PCI-E x8 Slimline Connector (G0) (J27)
44	PCI-E x8 Slimline Connector (G0) (J32)
45	PCI-E x8 Slimline Connector (G1) (J26)
46	PCI-E x4 Slimline Connector (P0) (J31)
47	System Battery (BH1)
48	RTC Connector (J56)
49	CPLD JTAG connector (J55)
50	M.2 Connector (J51)
51	M.2 Connector (J72)
52	PCI-E X16 Gen3 Slot2 (J28)
53	PCI-E X16 Gen3 Slot3 (J29)
54	VRD I^2C Connector (J115)

1.6.3 Front View

The system supports up to 8 2.5” HDDs. The front view of this 2U server allows easy access to HDDs. In addition, the front panel with buttons and system LEDs is located on the front.

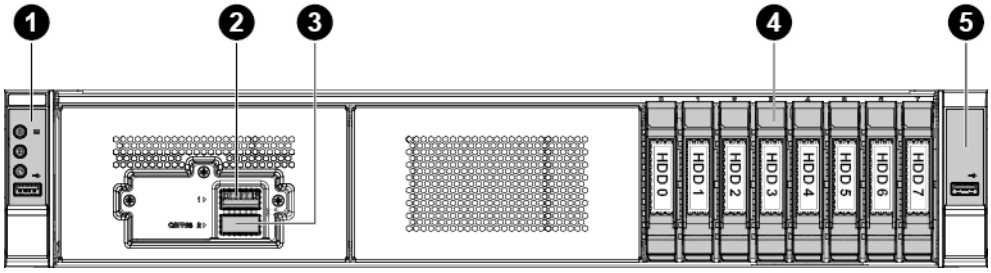


Figure 1-6 Front View with OCP Card

1	Front Panel 1
2	QSFP Port 1
3	QSFP Port 2
4	HDDs
5	Front Panel 2

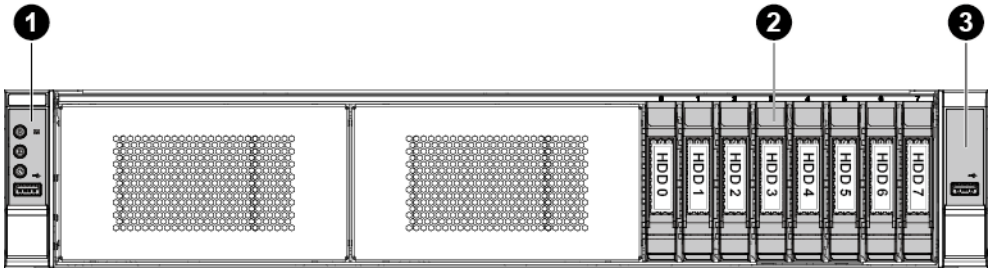


Figure 1-7 Front View

1	Front Panel 1
2	HDDs
3	Front Panel 2

1.6.4 Back View

The server back view includes the connectors of the external system devices.

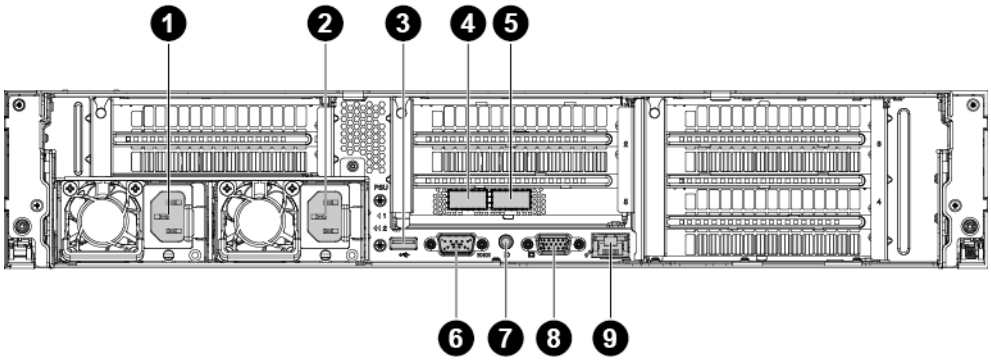


Figure 1-8 Back View

1	AC Power Connector 2
2	AC Power Connector 1
3	Rear Single USB Port
4	QSFP Port 1
5	QSFP Port 2
6	Serial Port (For BMC debug use only)
7	UID Button
8	VGA Connector
9	Management Port

1.6.5 Buttons and System LED Information

This server is equipped with system LED indicators, and buttons located on the front panels. The front panel status LEDs allow constant monitoring of basic system functions while the server is operating. These LEDs provide visual cues to the status of power and ID of motherboard.

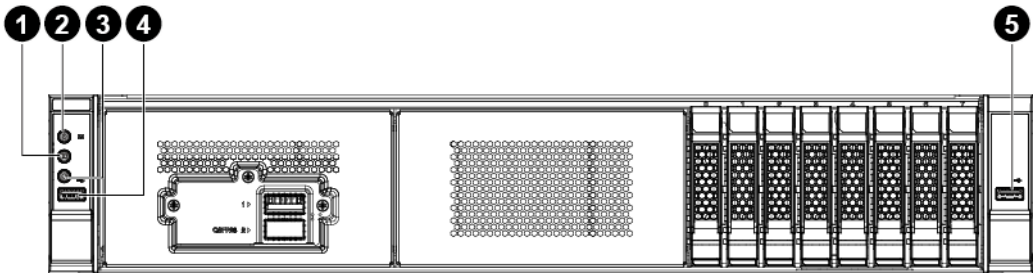


Figure 1-9 Front Panel Buttons and LEDs with OCP Card

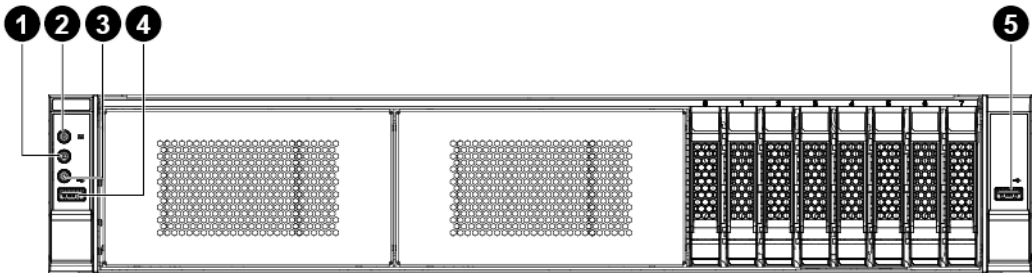


Figure 1-10 Front Panel Buttons and LEDs

1	ID Button/LED
2	Power Button/LED
3	Reset Button
4	USB 3.0 Port 0
5	USB 3.0 Port 1

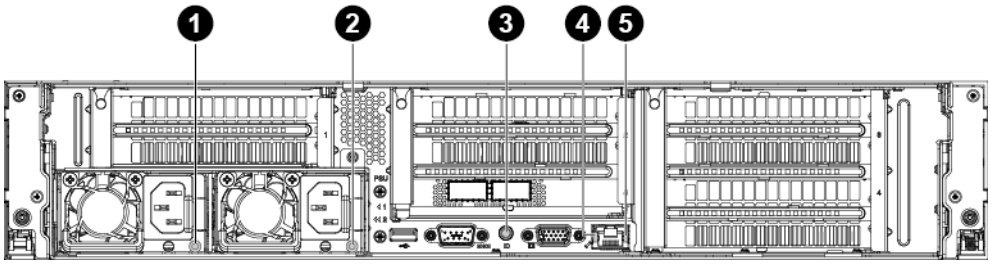


Figure 1-11 Back View LEDs

1	AC Power LED 2
2	AC Power LED 1
3	UID LED
4	Speed LED of Management Port
5	Link/Activity LED of Management Port

The detailed LED information is shown below:

Table 1-5 LED Information

Front View LEDs			
LED Type	**Color**	**Status**	**Function**
Power LED	Green	On	System is powered on. (S0, DC on)
	Amber	On	System is powered off. (S5, DC off)
	-	Off	AC power is disconnected.
ID LED	Blue	On	ID LED is turned on by BMC.
		Blinking	Unit selected for identification via software.
	-	Off	ID LED is off as Default.
System Health LED	Green	On	System is ready and in normal operation.
	Red	On	Non-recoverable failure, e.g. ● Non-recoverable temperature/voltage threshold, ● VRD hot asserted, ● Minimum number of fans does not present or failed. It could last even when power off.
		Blinking	Critical alarm, e.g. ● Critical temperature/voltage threshold, ● Power fault It could last even when power off.
	-	Off	AC power is disconnected or system power off in normal.
Back View LEDs			
LED Type	**Color**	**Status**	**Function**
AC Power LED	Green	On	Output is ON and works normally.
		Blinking (0.5Hz)	Standby mode is normal.
		Blinking (2Hz)	Sleep PSU is in cold redundant and in offline mode.

	Amber	On	• Standby mode with OTP range • 12V Fault (include: OVP, UVP, OCP, SCP, and OTP). • Fan locks 15 seconds including standby mode.
	-	Off	No AC power.
Speed LED of Base-T port 0/1	Green	On	Link at first level speed.
	Amber	On	Link at others speeds.
	-	Off	No link.
Link/Activity LED of Base-T port 0/1	Green	On	Link ON without accessing
		Blinking	Link ON with accessing
	-	Off	No link.

1.6.6 System Thermal Solution

This server provides a thermal solution to keep proper cooling. The components in the following figure must be installed in place.

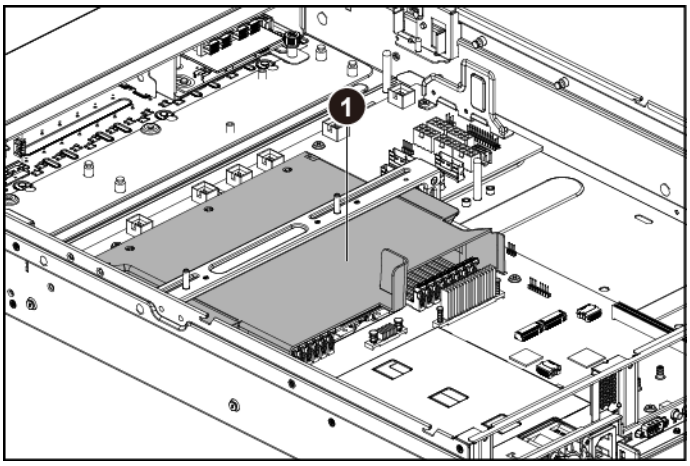


Figure 1-12 Thermal Solution

1	Fan Duct

Chapter 2
Hardware Operations

Before You Start
Rear Chassis Cover
Front Top Cover
Cable Guide
Stiffener
Motherboard
Power Supplies
System Fans
2.5” HDDs
8x2.5” HDD Backplane
Front Panels
OCP Card
Expansion Cards
Fan Duct

2 Hardware Operations

This chapter describes the hardware setup procedures that you have to perform when replacing system components. It also gives detailed information on the internal components and how to replace them.

The components shown in this chapter are mainly for your reference. Please take the actual shipment as standard.

2.1 Before You Start

Take note of the following operations before you start to remove or install internal components.

2.1.1 Power Off

To reduce the risk of injury from electric shock, remove the power cord to completely disconnect power from the system.

Moving the Power On/Off switch to the Off position does not completely remove power from the system. Some portions of the power supply and some internal circuitry remain active. Disconnect all power cords from the server to completely remove power from the system.

To press the power button:

Press the power button ❶ to toggle the server to standby. The power LED ❶ in green turns off.

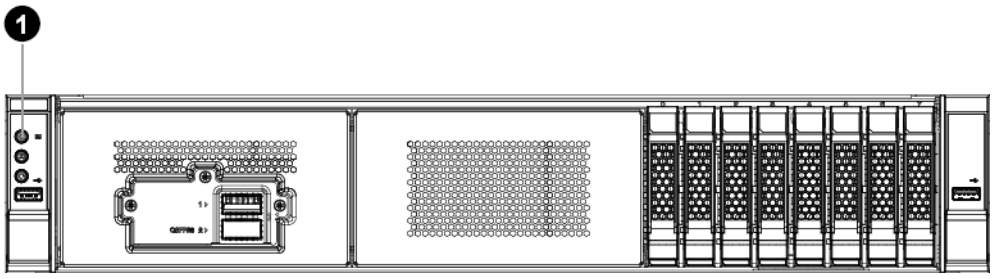


Figure 2-1 Pressing the Power Button

To remove the power cords:

First unplug the power cords from the AC outlet and then from the server.

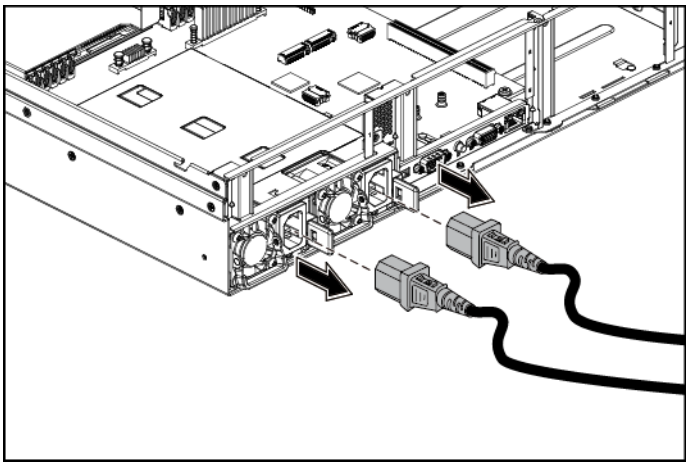


Figure 2-2 Unplugging the Power Cords

2.2 Rear Chassis Cover

The server is a 2U form factor designed for easy assembly and disassembly, making the replacement of internal components very convenient.

Reminder

Before you remove or install the rear chassis cover, please follow the step below:

Step 1: *Make sure the server is not turned on or connected to the AC power. To power off the server, see "2.1.1 Power Off".*

2.2.1 To remove the rear chassis cover

❶ Release the screw on the chassis cover.

❷ Push the retaining clip along the direction of the arrow.

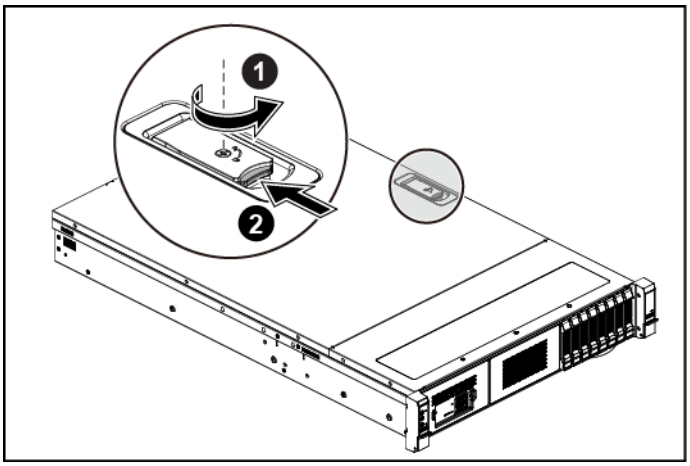


Figure 2-3 Releasing the Chassis Cover

❸ Pull up the retaining clip completely to the biggest angle.
❹ Simultaneously the cover automatically slides backward.
❺ Remove the cover from the chassis.

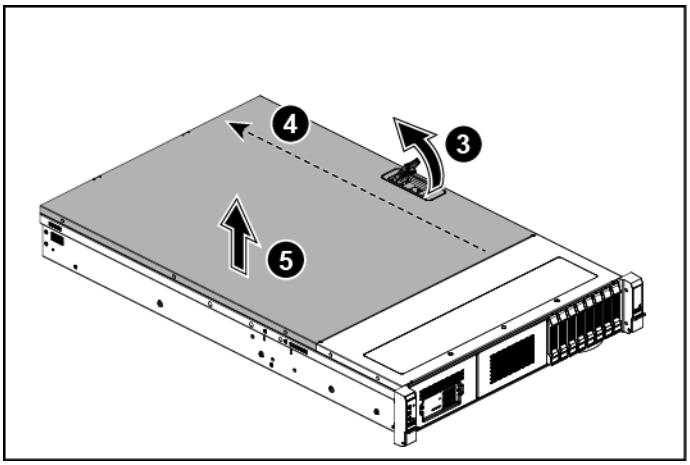


Figure 2-4 Removing the Chassis Cover

2.2.2 To install the rear chassis cover

❶ Locate the chassis cover onto the chassis.
❷ Simultaneously pull up the retaining clip completely with the biggest angle, and align the locking tabs on the cover to the corresponding notches on the chassis.

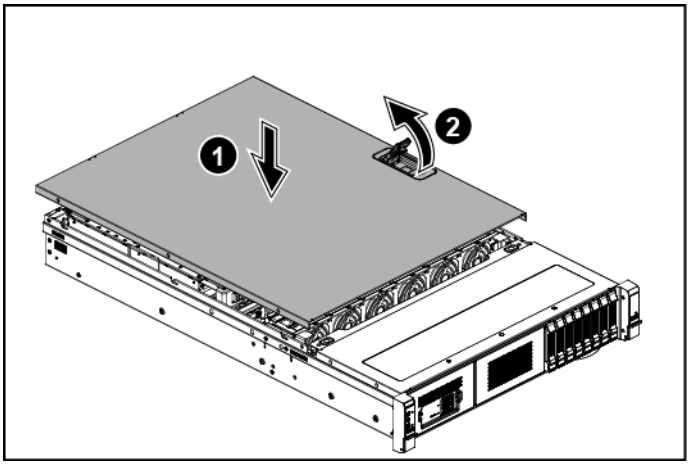


Figure 2-5 Locating the Cover onto the Chassis

❸ Secure the retaining clip and simultaneously the cover automatically slides back into place.

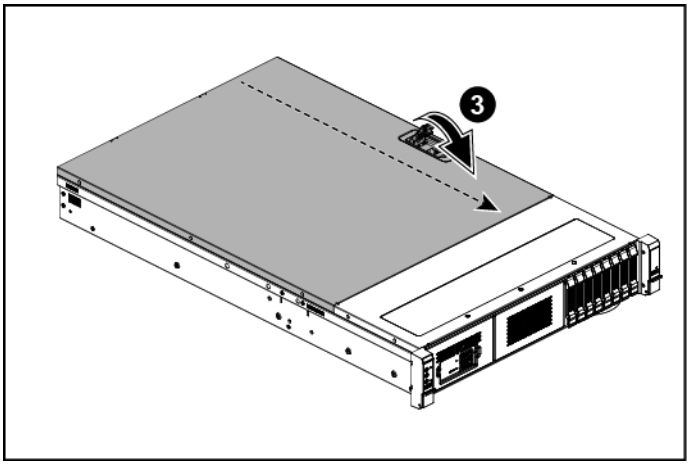


Figure 2-6 Secure the retaining clip

❸ Secure the chassis cover with one screw.

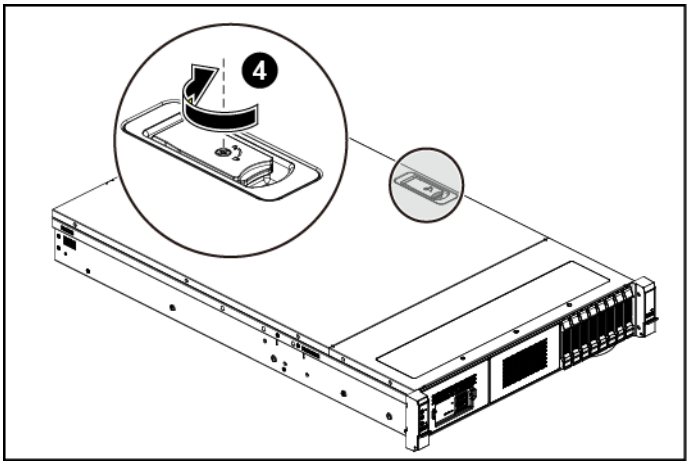


Figure 2-7 Tightening the Screw

This system must be operated with the chassis cover installed to ensure proper cooling.

2.3 Front Top Cover

The server is a 2U form factor designed for easy assembly and disassembly, making the replacement of internal components very convenient.

Reminder

Before you remove or install the front top cover, please follow the step below:

Step 1: *Make sure the server is not turned on or connected to the AC power. To power off the server, see "2.1.1 Power Off".*

Step 2: *Remove the rear chassis cover. To remove the rear chassis cover, see"2.2 Rear Chassis Cover".*

2.3.1 To remove the front top cover

❶ Press down the retaining clip.

❷ Remove the front top cover along the direction of the arrow.

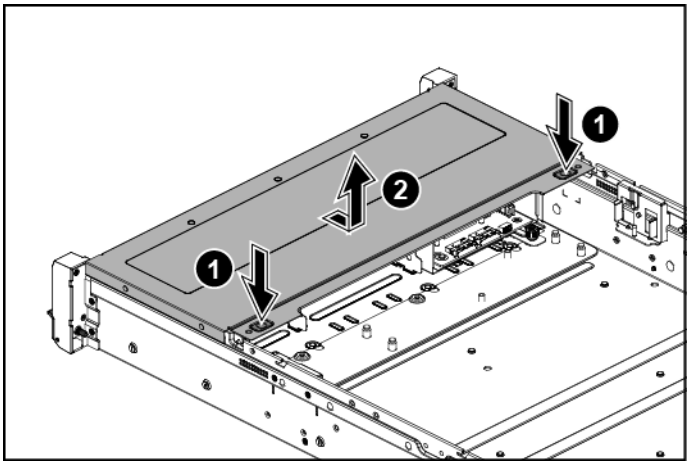


Figure 2-8 Removing the Front Top Cover

2.3.2 To install the front top cover

Locate the front top cover onto the chassis with the locking tabs on the cover snap into the corresponding notches on the chassis.

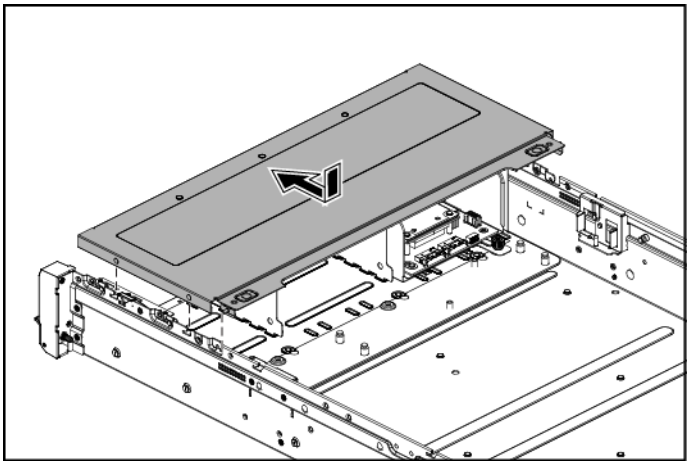


Figure 2-9 Installing the Front Top Cover

This system must be operated with the chassis cover installed to ensure proper cooling.

2.4 Cable Guide

The locations of cable guide on the server is shown below:

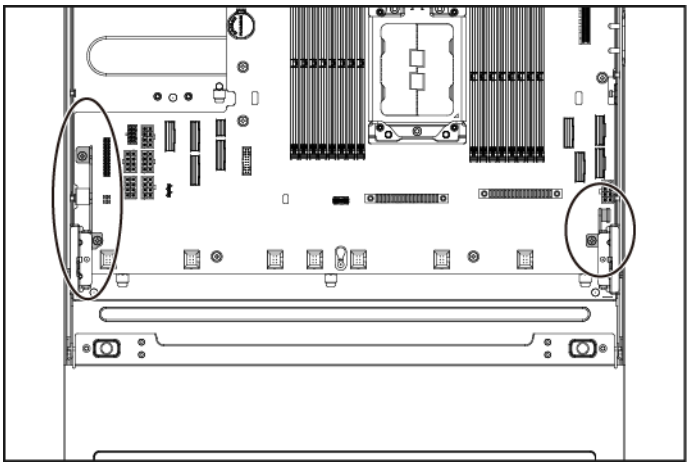


Figure 2-10 Cable Guide Location

Reminder

Before you remove or install the cable guide, please follow the steps below:

Step 1: *Make sure the server is not turned on or connected to the AC power. To power off the server, see "2.1.1 Power Off"*

Step 2: *Remove the rear chassis cover. To remove the rear chassis cover, see"2.2 Rear Chassis Cover".*

Step 3: *Remove the fan duct. To remove the fan duct, see "2.16 Fan Duct".*

Step 4: *Disconnect all necessary cables.*

2.4.1 To remove the cable guide

❶ Remove the two screws that secure the cable guide.

❷ Lift the cable guide out of the chassis.

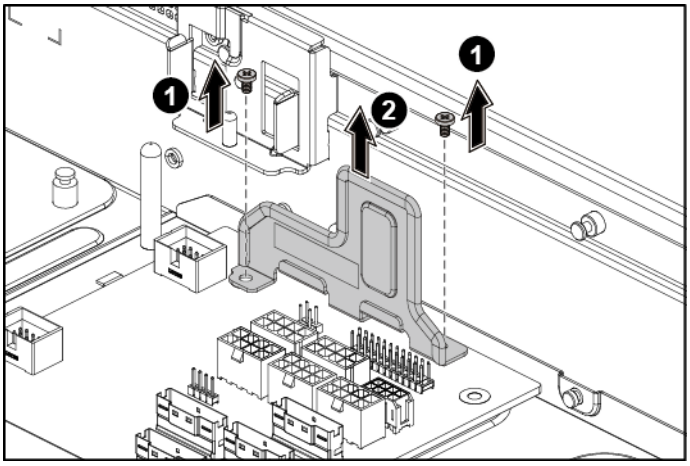


Figure 2-11 Removing the Cable Guide

2.4.2 To install the cable guide

Reverse the steps above to install the cable guide.

2.5 Stiffener

The locations of stiffener on the server is shown below:

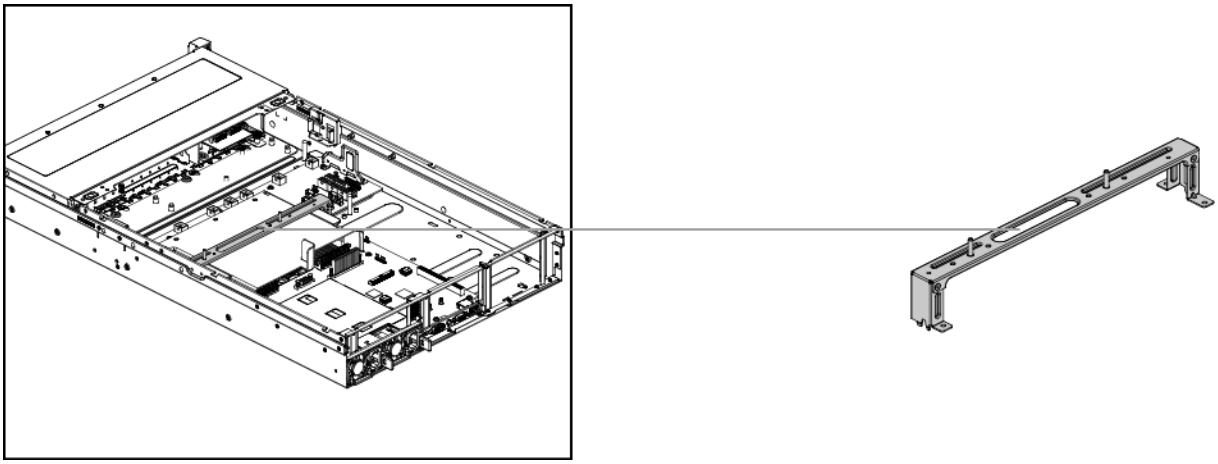


Figure 2-12 Stiffener Location

Reminder

Before you remove or install the stiffener, please follow the steps below:

Step 1: *Make sure the server is not turned on or connected to the AC power. To power off the server, see "2.1.1 Power Off"*

Step 2: *Remove the rear chassis cover. To remove the rear chassis cover, see"2.2 Rear Chassis Cover".*

Step 3: *Remove the fan duct. To remove the fan duct, see "2.16 Fan Duct".*

2.5.1 To remove the stiffener

❶ Release the screws.

❷ Lift the stiffener out of the chassis.

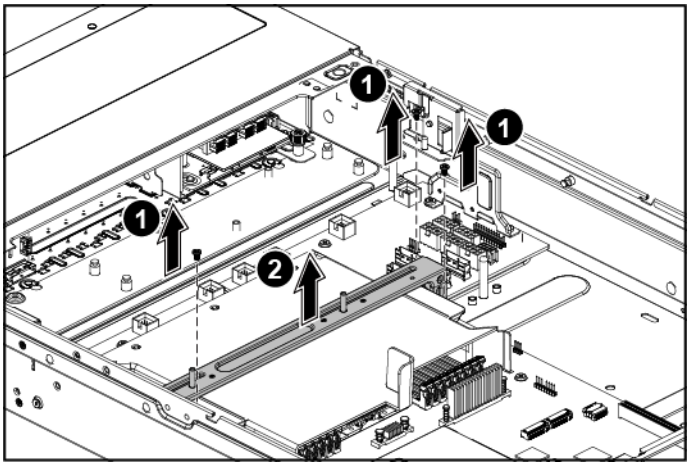


Figure 2-13 Removing the Stiffener

2.5.2 To install the stiffener

Reverse the steps above to install the stiffener.

2.6 Motherboard

The location of motherboard on the server is shown below:

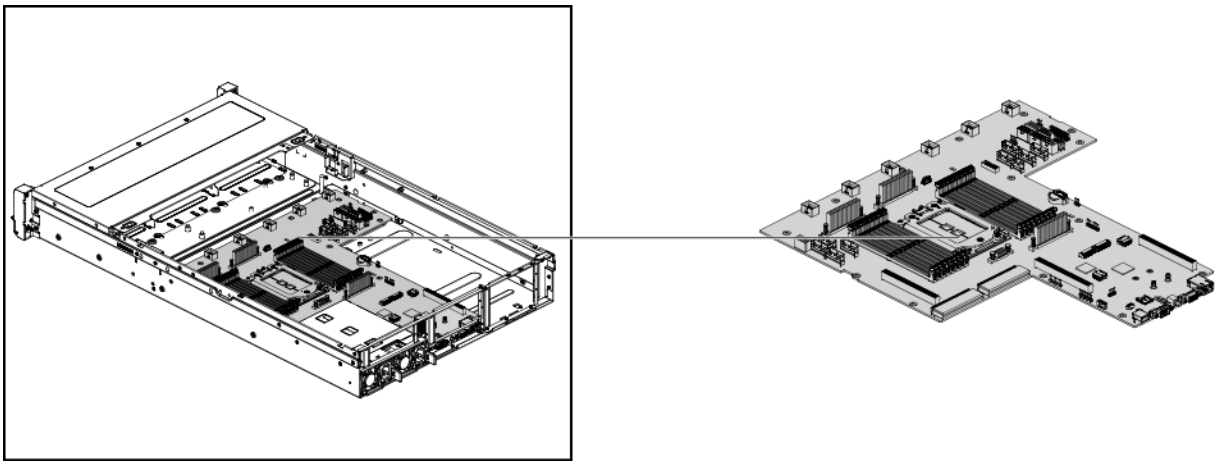


Figure 2-14 Motherboard Location

Reminder

Before you remove or install the motherboard, please follow the steps below:

Step 1: *Make sure the server is not turned on or connected to the AC power. To power off the server, see "2.1.1 Power Off"*

Step 2: *Remove the rear chassis cover. To remove the rear chassis cover, see"2.2 Rear Chassis Cover".*

Step 3: *Remove the fan duct. To remove the fan duct, see "2.16 Fan Duct".*

Step 4: *Remove the stiffener. To remove the stiffener see "2.5 Stiffener".*

Step 5: *Remove the cable guide. To remove the cable guide, see "2.4 Cable Guide".*

Step 6: *Disconnect all necessary cables.*

2.6.1 To remove the motherboard

❶ Release the retaining clip that secure the system fan cage.
❷ Lift the system fan assembly out of the chassis.

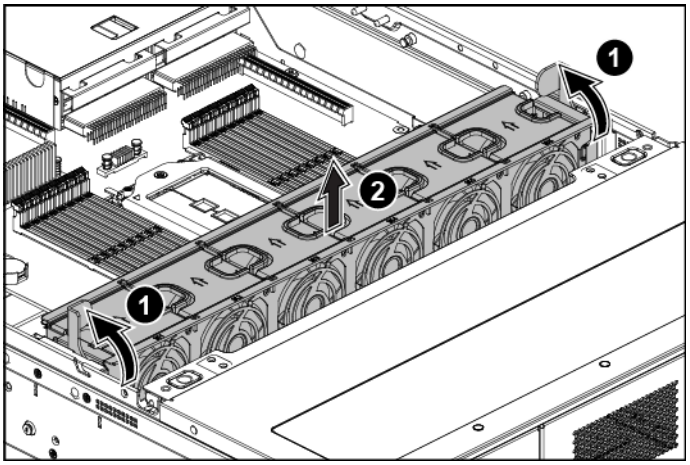


Figure 2-15 Removing the System Fan Assembly

❸ Remove the 8 screws that secure the motherboard.
❹ Remove the motherboard out of the chassis along the direction of the arrow.

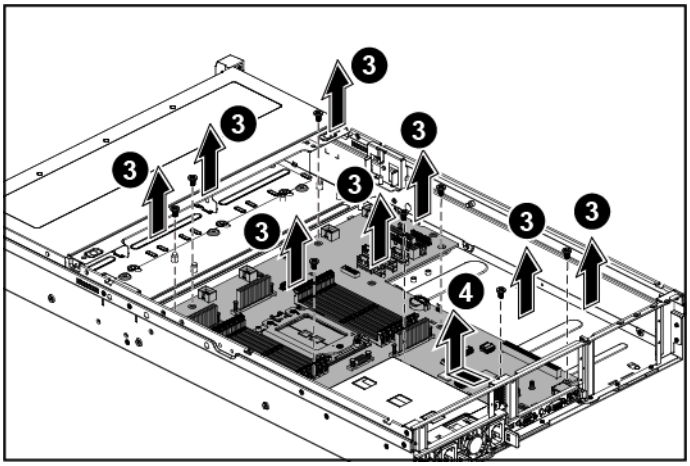


Figure 2-16 Removing the Motherboard

2.6.2 To install the motherboard

Reverse the steps above to install the motherboard.

2.7 Processor

This motherboard supports one AMD Naples SP3 processor.

The location of processor on the motherboard is shown below:

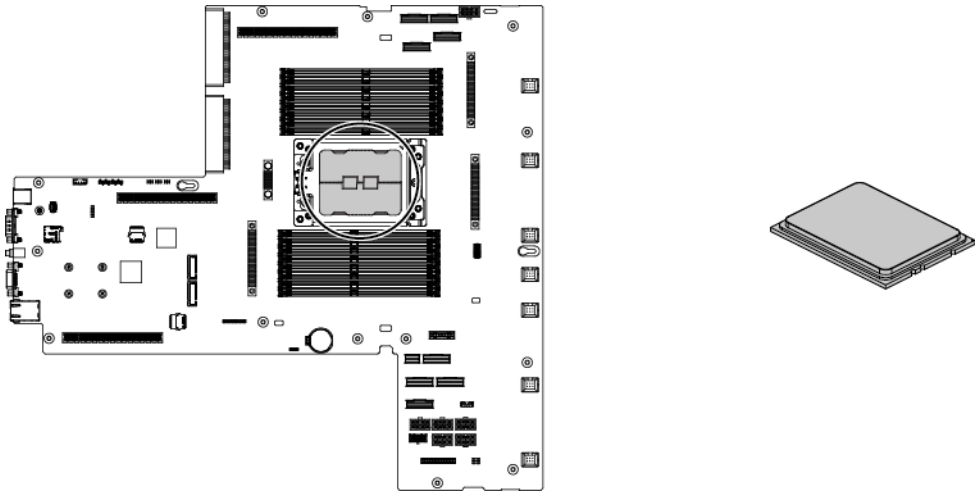


Figure 2-1 Location of Processor

Reminder

Before you remove or install the processor, please follow the steps below:

Step 1: *Make sure the server is not turned on or connected to the AC power. To power off the server, see "2.1.1 Power Off"*

Step 2: *Remove the rear chassis cover. To remove the rear chassis cover, see"2.2 Rear Chassis Cover".*

Step 3: *Remove the fan duct. To remove the fan duct, see "2.16 Fan Duct".*

Step 4: *Remove the stiffener. To remove the stiffener see "2.5 Stiffener".*

Step 5: *Remove the cable guide. To remove the cable guide, see "2.4 Cable Guide".*

Step 6: *Disconnect all necessary cables.*

2.7.1 To remove the heat sink

The heat sink used in the figure below is just for your reference. Please choose an appropriate heat sink depending on the whole system requirement.

❶ Loosen the four securing screws.
❷ Lift the heat sink up from the installed processor.

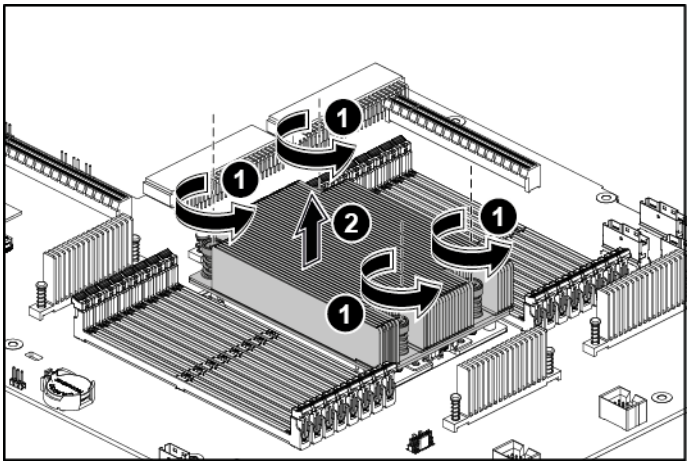


Figure 2-2 Removing the Heat Sink

2.7.2 To install the heat sink

Reverse the steps above to install the heat sink.

Before you put the heat sink on top of the installed processor, please do not forget to check if the grease is complete on bottom of the heat sink.

2.7.3 To remove the processor

❶ Remove the screw marked with “3” around it.
❷ Remove the screw marked with “2” around it.
❸ Remove the screw marked with “1” around it.

To release the force frame, you must remove the screws following the sequence of “3”, “2” and “1” marked around them.

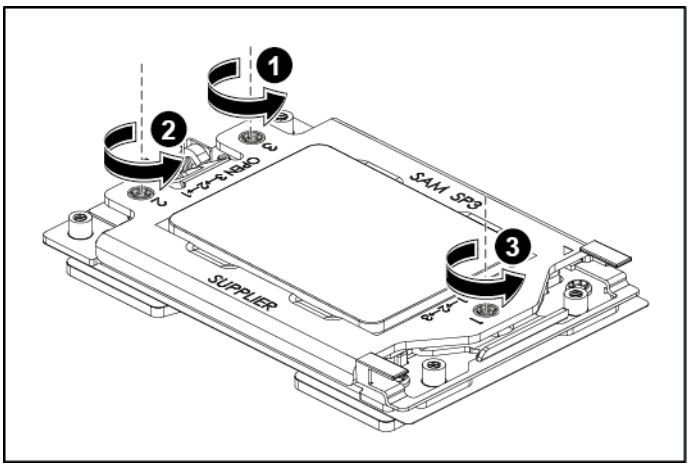


Figure 2-3 Releaing the Force Frame

❹ Open the force frame.
❺ Hold the two clips of the rail frame and lift them up.

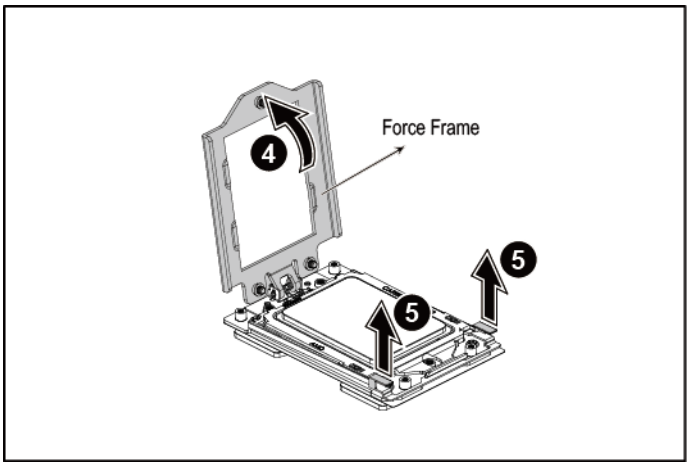


Figure 2-4 Opening the Force Frame

❻ Open the rail frame.

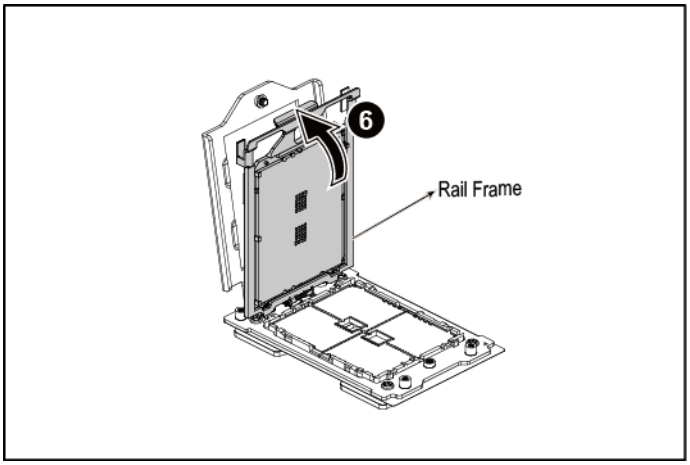


Figure 2-5 Opening the Rail Frame

❼ Pull the CPU package out of the rail frame.

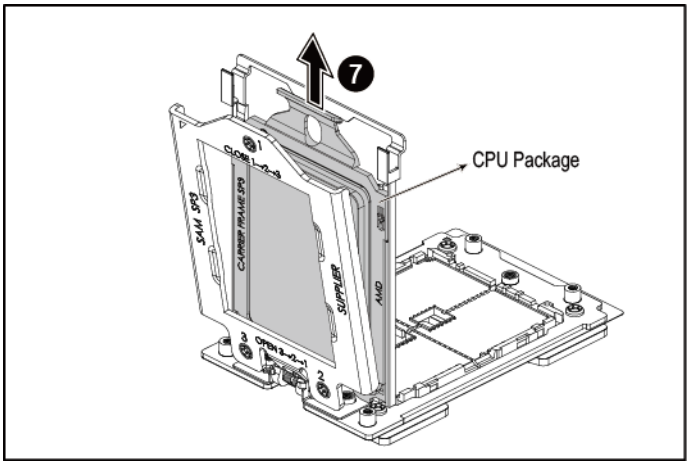


Figure 2-6 Removing the CPU Package

2.7.4 To install the processor

Reverse the steps above to install the processor.

- When installing the CPU package, make sure to hold the handle but not the processor.
- To secure the force frame, you must install the screws following the sequence of “1”, “2” and “3” marked around them.

2.8 System Memory

This motherboard supports sixteen DDR4 1866/2133/2400/2667 ECC registered DIMM/RDIMM.

The locations of the DIMM sockets on the motherboard is shown below:

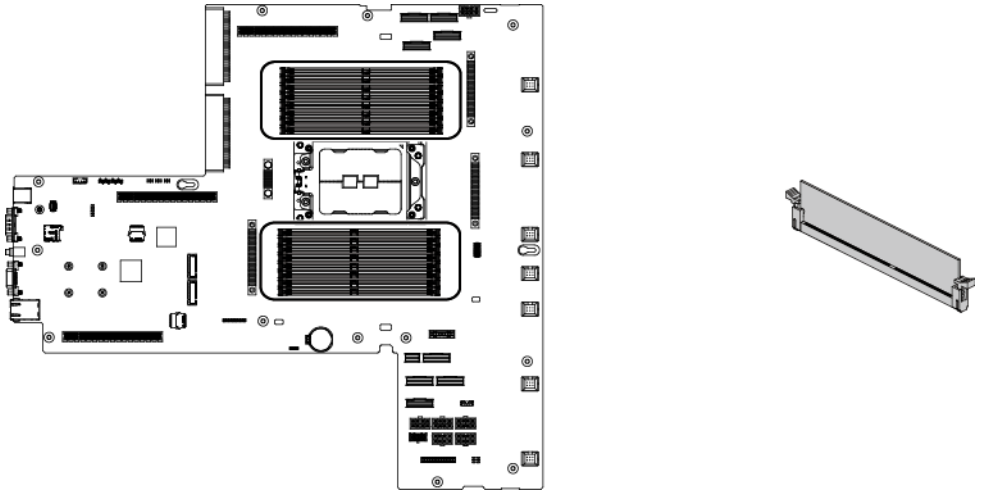


Figure 2-7 Locations of System Memories

Reminder

Before you remove or install the system memory, please follow the steps below:

Step 1: *Make sure the server is not turned on or connected to the AC power. To power off the server, see "2.1.1 Power Off"*

Step 2: *Remove the rear chassis cover. To remove the rear chassis cover, see"2.2 Rear Chassis Cover".*

Step 3: *Remove the fan duct. To remove the fan duct, see "2.16 Fan Duct".*

Step 4: *Remove the stiffener. To remove the stiffener see "2.5 Stiffener".*

Step 5: *Disconnect all necessary cables.*

There are sixteen DIMMs on the motherboard to support the processor. The DIMM sequence of the sixteen DIMM sockets is respectively shown below.

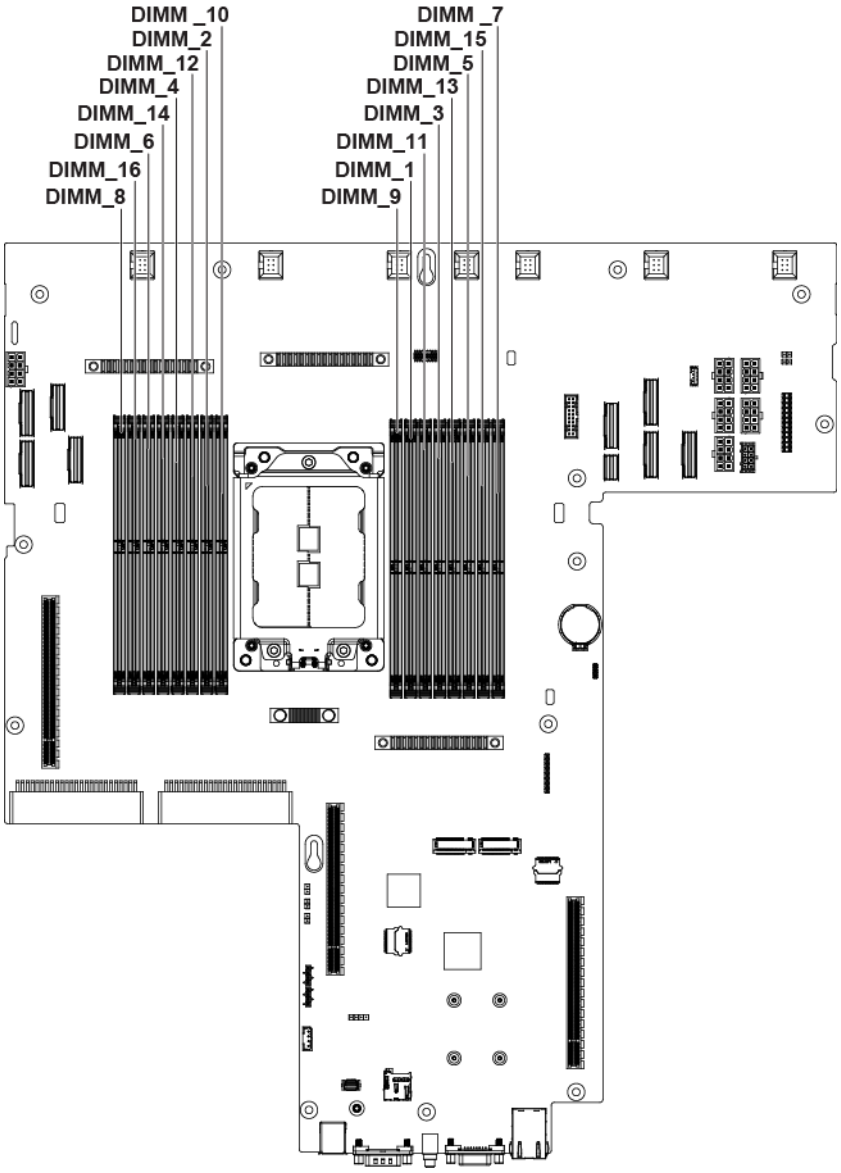


Figure 2-8 DIMM Socket Sequence

2.8.1 To remove the system memory

❶ Unlock a DIMM socket by pressing the retaining clips outward. This action releases the module and partially lifts it out of the socket.
❷ Lift out the DIMM.

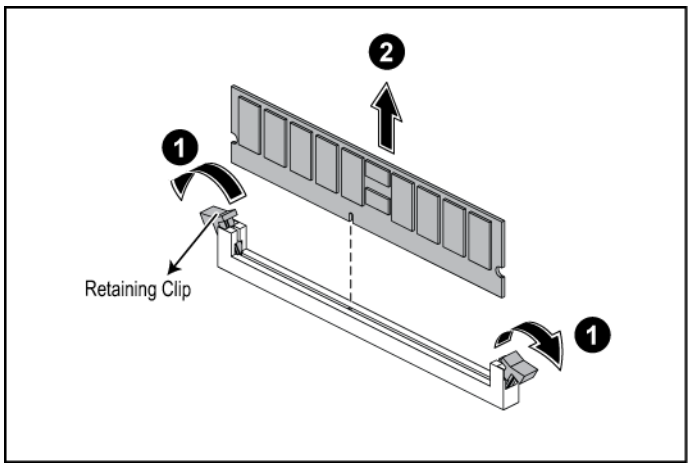


Figure 2-9 Lifting the DIMM out of the Socket

2.8.2 To install the system memory

❶ Unlock a DIMM socket by pressing the retaining clips outward.

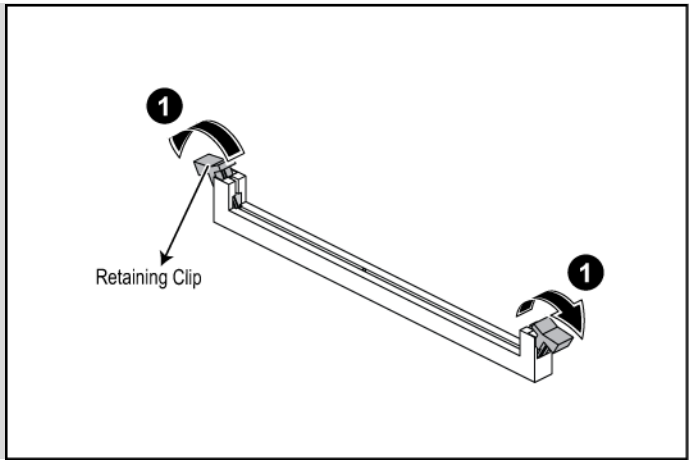


Figure 2-10 Pressing the Retaining Clips Outward

❷ Align the notch on the DIMM to the break on the socket. Carefully insert the DIMM into the socket until the retaining clips snap back in place.

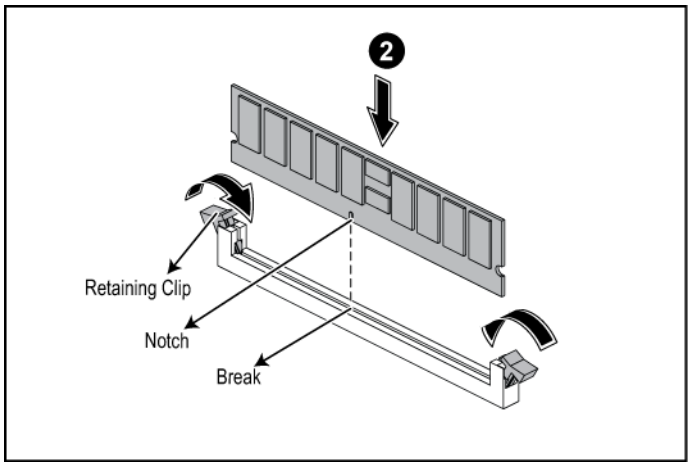


Figure 2-11 Inserting the DIMM into the Socket

DIMMs fit in only one direction. DO NOT force a DIMM into the socket to avoid damaging the DIMM.

2.9 Power Supplies

This server is designed with single 1600W/2000W power supply or two 1600W/2000W redundant power supplies with system throttling mode.

The location of power supplies on the server is shown below:

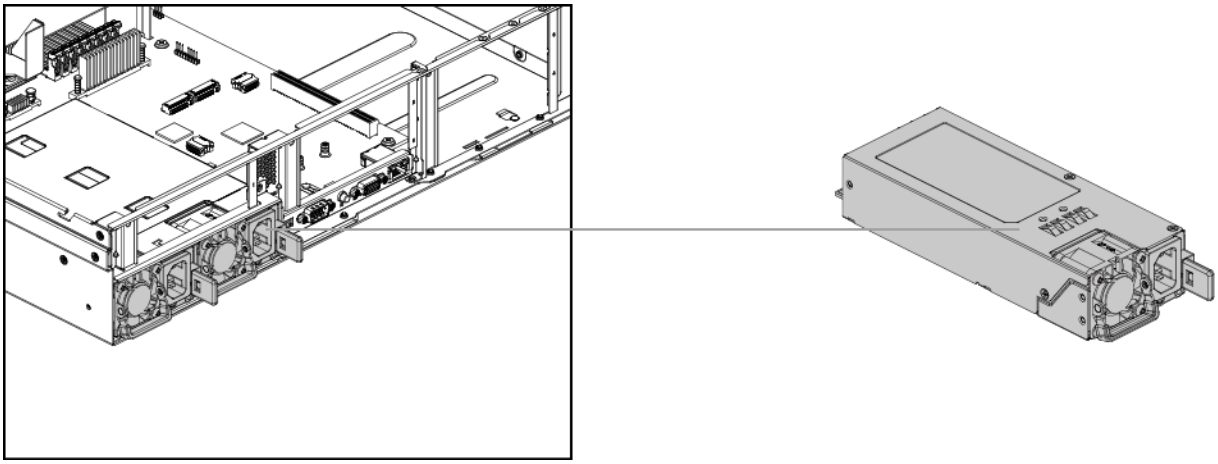


Figure 2-17 Power Supply Locations

Reminder

Before you remove or install the power supply, please follow the steps below:

Step 1: *Disconnect all necessary cables.*

2.9.1 To remove the power supply

❶ Press the retaining clip on the right side of the power supply along the direction of the arrow.

❷ Pull down the power supply handle.

❸ At the same time, pull out the power supply. (The power supply takes considerable force to remove.)

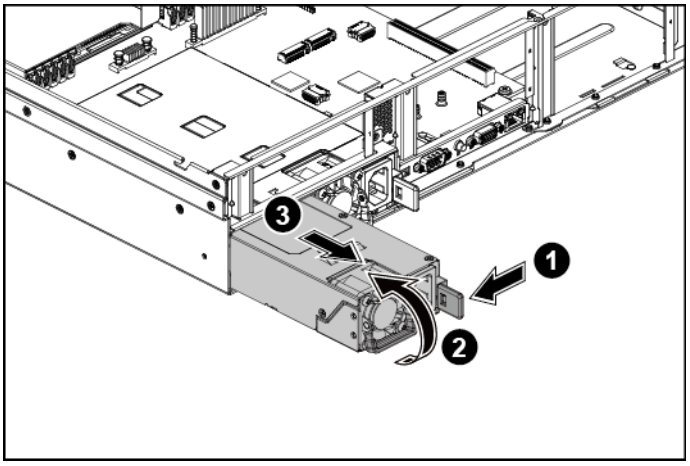


Figure 2-18 Removing the Power Supply

2.9.2 To install the power supply

Insert the replacement power supply firmly into the bay. The retaining clip should snap. Connect the AC power cord to the replacement power supply.

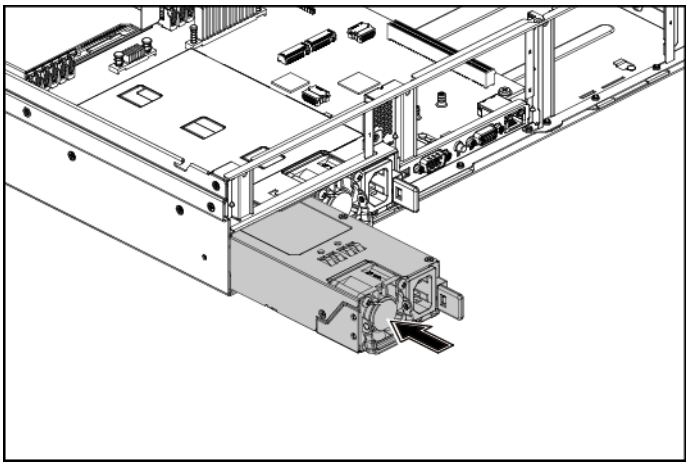


Figure 2-19 Installing the Power Supply

2.10 System Fans

Subdividing the motherboard area and the backplane area is a metal cage that holds the system fans. This server contains 6 system fans which are located inside the chassis. These system fans maintain the ideal temperature for the motherboard, backplane and disk drives.

The location of system fans is shown below:

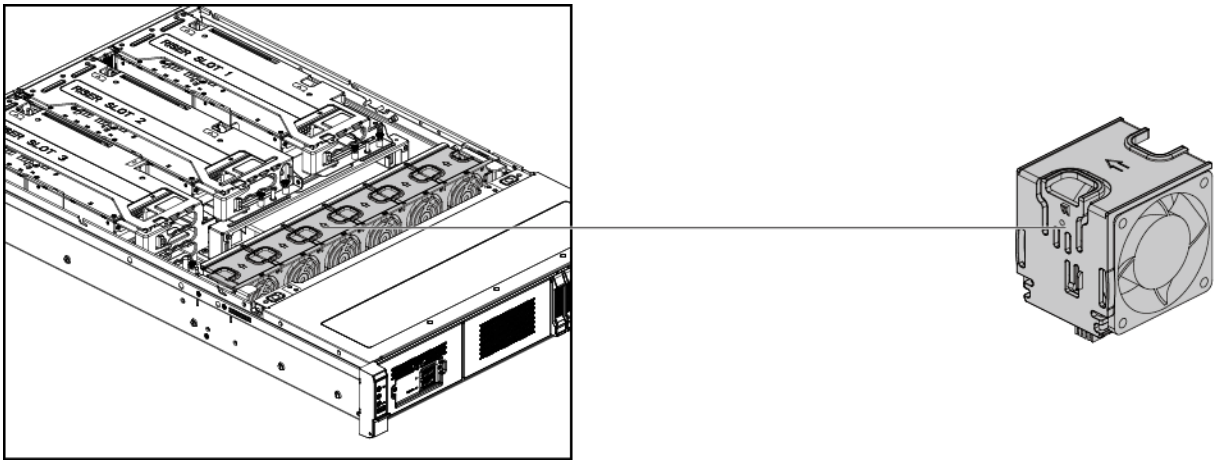


Figure 2-20 System Fan Locations

Reminder

Before you remove or install the system fan, please follow the steps below:

Step 1: *Make sure the server is not turned on or connected to the AC power. To power off the server, see "2.1.1 Power Off"*

Step 2: *Remove the rear chassis cover. To remove the rear chassis cover, see"2.2 Rear Chassis Cover".*

Step 3: *Disconnect all necessary cables.*

2.10.1 To remove the system fans

❶ Unlock the system fan by clamping the locking clip inward.
❷ Take the system fan out of the system fan cage.

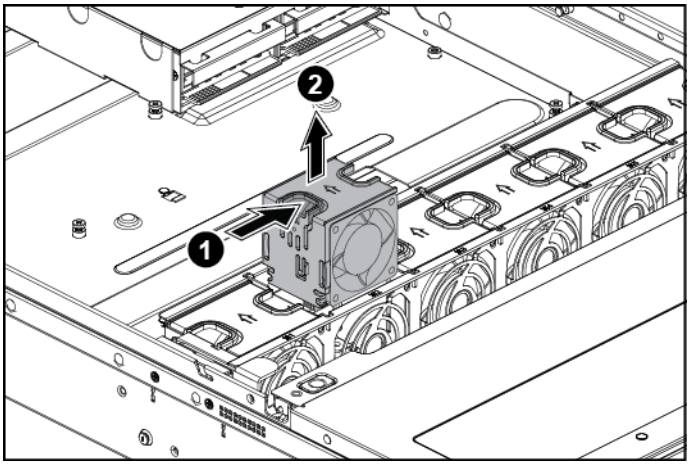


Figure 2-21 Removing the System Fan

2.10.2 To install the system fans

Place the system fan into the system fan cage.

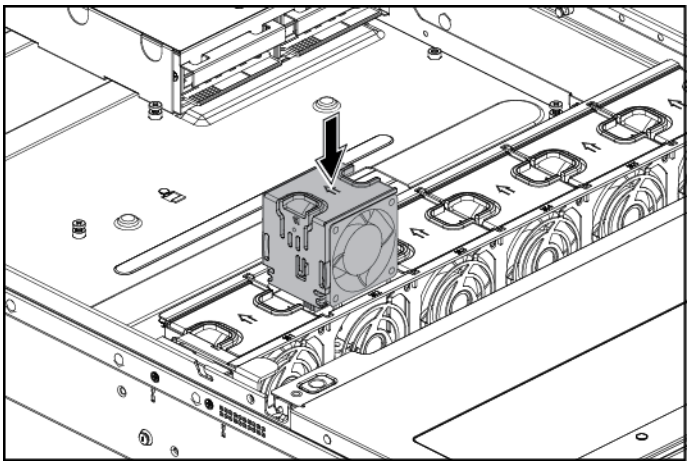


Figure 2-22 Installing the System Fan

2.11 2.5” HDDs

The server can support 8x2.5” hot-pluggable HDDs. Each HDD is with an adapter bracket. You don’t need to power-off the system when removing or installing a HDD.

The location of the 2.5” HDDs on the server is shown below:

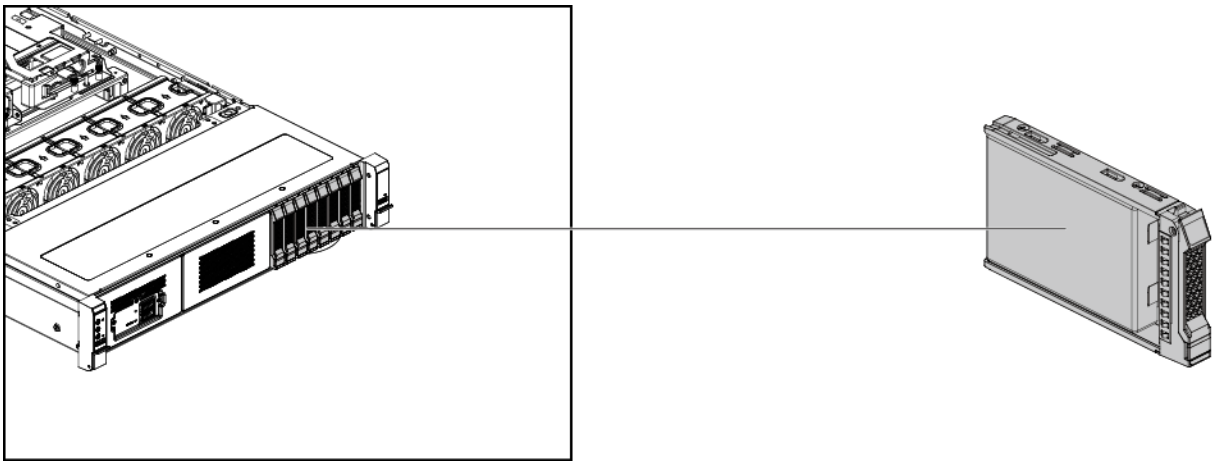


Figure 2-23 2.5” HDD Locations

- Take note of the drive tray orientation before sliding it out.
- The tray will not fit back into the bay if inserted incorrectly.

2.11.1 To remove the 2.5” HDD

❶ Push the release button.
❷ Pull the lever open.
❸ Slide the HDD assembly out of the HDD bay.

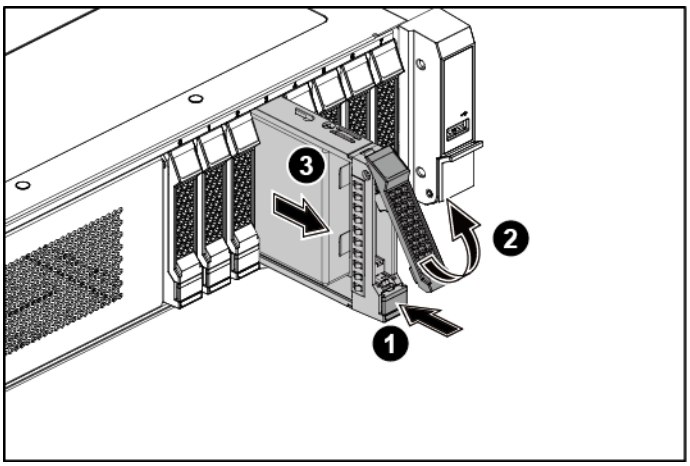


Figure 2-24 Sliding out the 2.5” HDD Assembly

❹ Lift the HDD out of the tray.

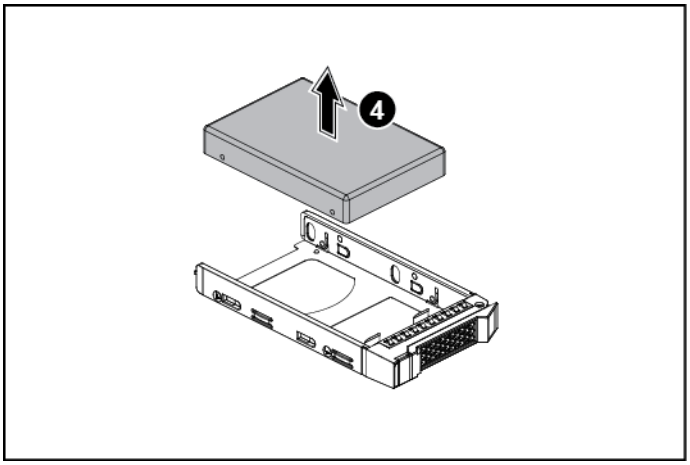


Figure 2-25 Removing the HDD

2.11.2 To install the 2.5” HDD

❶ Place the HDD to the HDD tray.

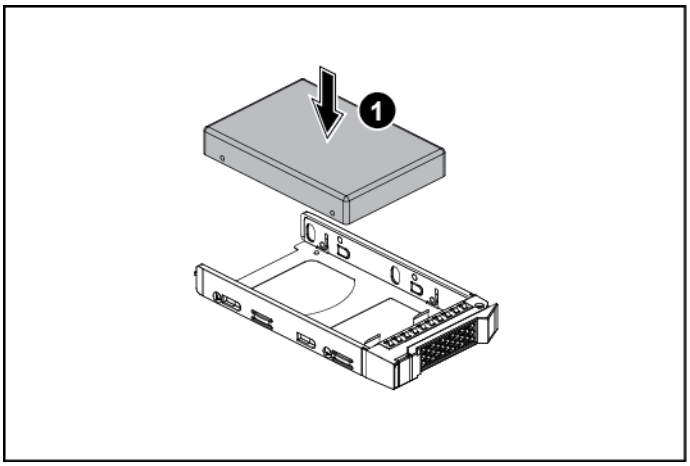


Figure 2-26 Placing the HDD

❷ Carefully insert the HDD assembly into the HDD bay with the lever lifted until it completely enters the HDD bay.

❸ Push the lever back in place.

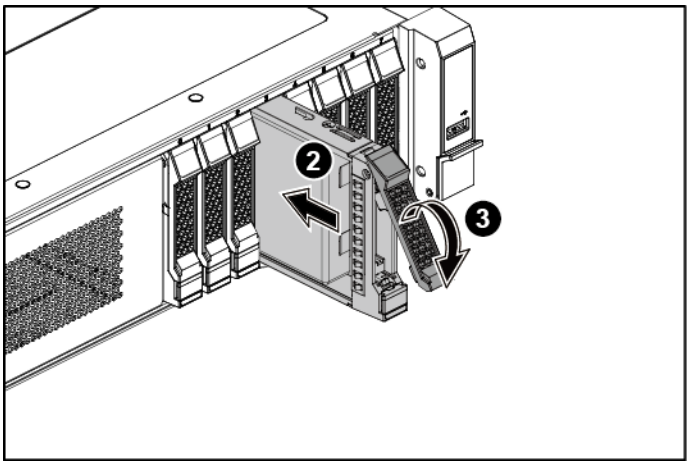


Figure 2-27 Installing the HDD Assembly

Make sure that the HDD is connected to the HDD connector on the backplane.

2.12 8x2.5” HDDs Backplane

The server supports one 8x2.5” HDDs backplanes, which can support up to eight 2.5” HDDs with adapter bracket in the system. The design incorporates a hot-swappable feature to allow easy replacement of HDDs. The SATA or SAS connectors on each backplane connect to the motherboard to provide power and indicate HDD access and failure.

The location of 8x2.5” HDDs backplane is shown below:

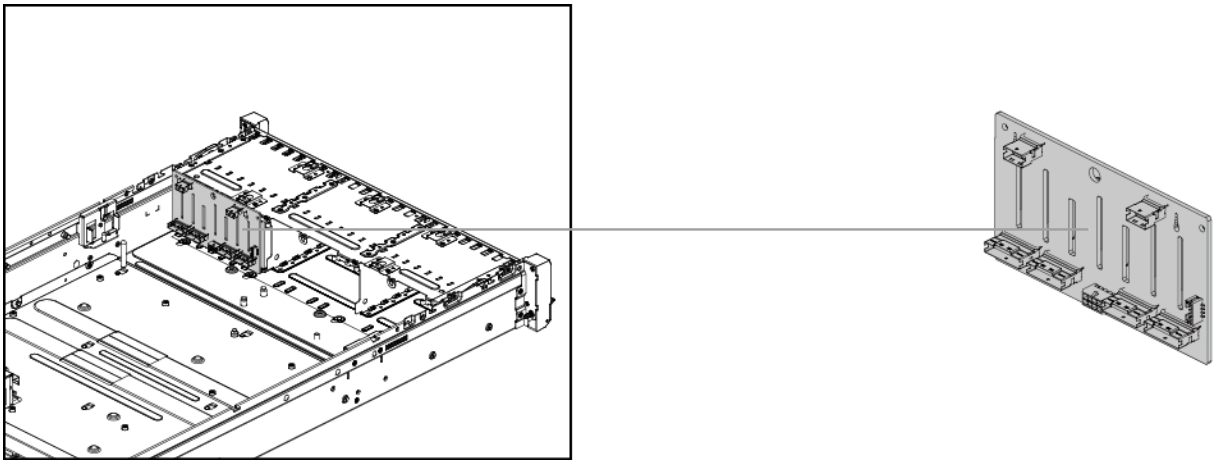


Figure 2-28 8x2.5” HDDs Backplane Location

Reminder

Before you remove or install the 8x2.5" HDDs backplane, please follow the steps below:

Step 1: *Make sure the server is not turned on or connected to the AC power. To power off the server, see "2.1.1 Power Off".*

Step 2: *Remove the rear chassis cover. To remove the rear chassis cover, see"2.2 Rear Chassis Cover".*

Step 3: *Remove the front top cover. To remove the front top cover, see "2.3 Front Top Cover".*

Step 4: *Remove the HDDs.To remove a HDD, see " 2.11 2.5" HDDs".*

Step 5: *Disconnect all the necessary cables.*

2.12.1 To remove the 8x2.5" HDDs backplane

❶ Remove the screws that secure the backplane.

❷ Remove the backplane along the direction of the arrow.

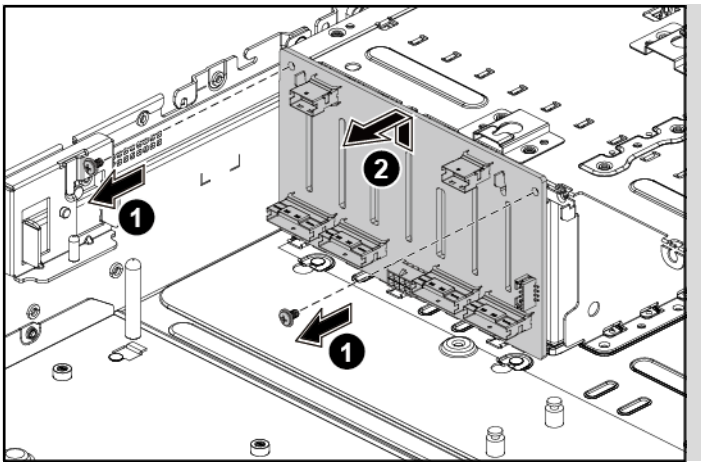


Figure 2-29 Removing the 8x2.5" HDDs backplane

2.12.2 To install the 8x2.5" HDDs backplane

Reverse the steps above to install the 8x2.5" HDDs backplane.

2.13 Front Panels

The location of left front panel on the server is shown below:

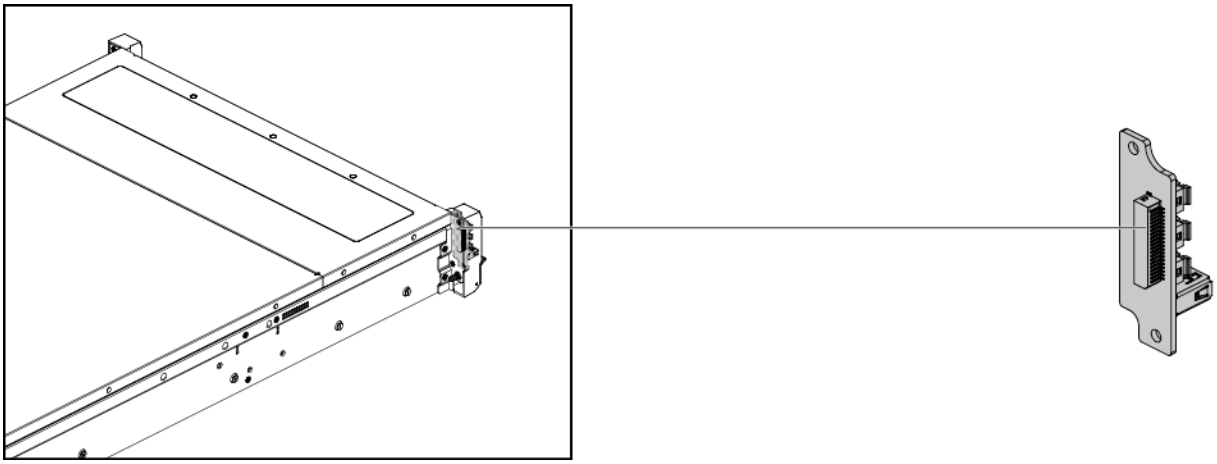


Figure 2-30 Left Front Panel Location

The location of right front panel on the server is shown below:

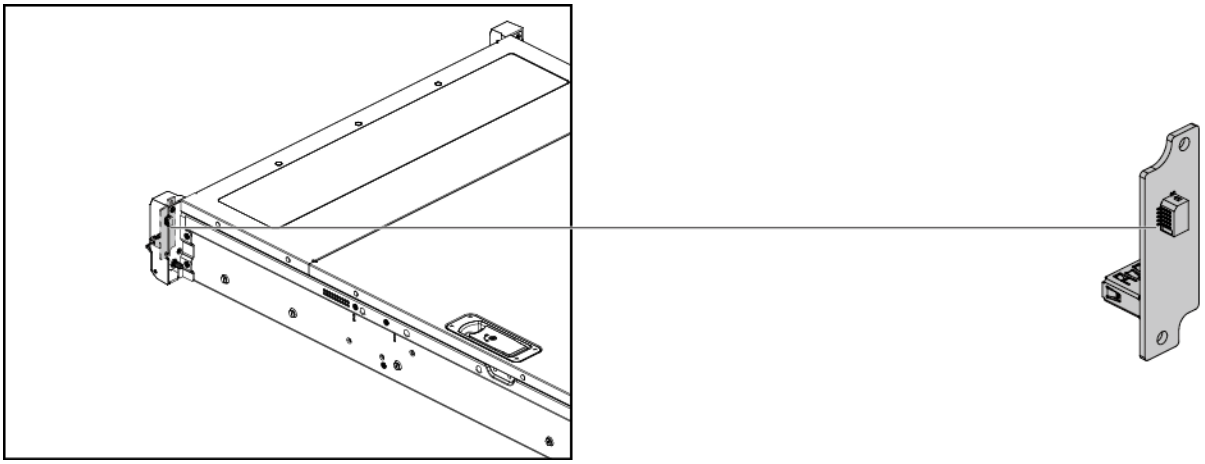


Figure 2-31 Right Front Panel Location

Reminder

Before you remove or install the front panel, please follow the steps below:

Step 1: *Make sure the server is not turned on or connected to the AC power. To power off the server, see "2.1.1 Power Off".*

2.13.1 To remove the front panel

❶ Unscrew the front panel assembly.
❷ Remove the front panel assembly from the chassis.

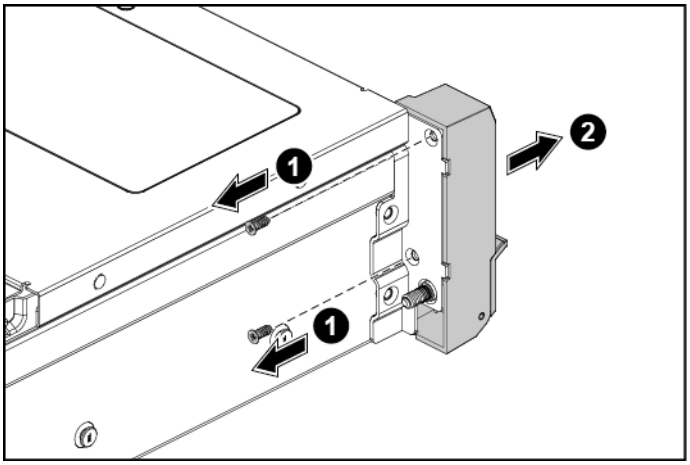


Figure 2-32 Removing the Front Panel Assembly

❸ Unscrew the front panel.
❹ Remove the front panel.

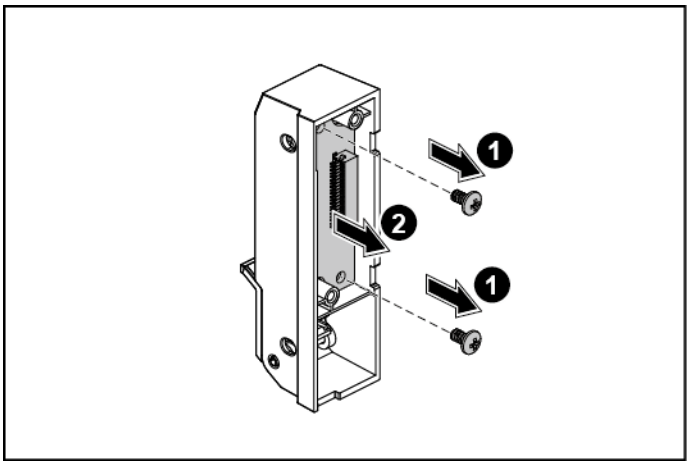


Figure 2-33 Removing the Front Panel

2.13.2 To install the front panel

Reverse the steps above to install the front panel.

2.14 OCP Card (Optional)

The location of OCP card on the server is shown below:

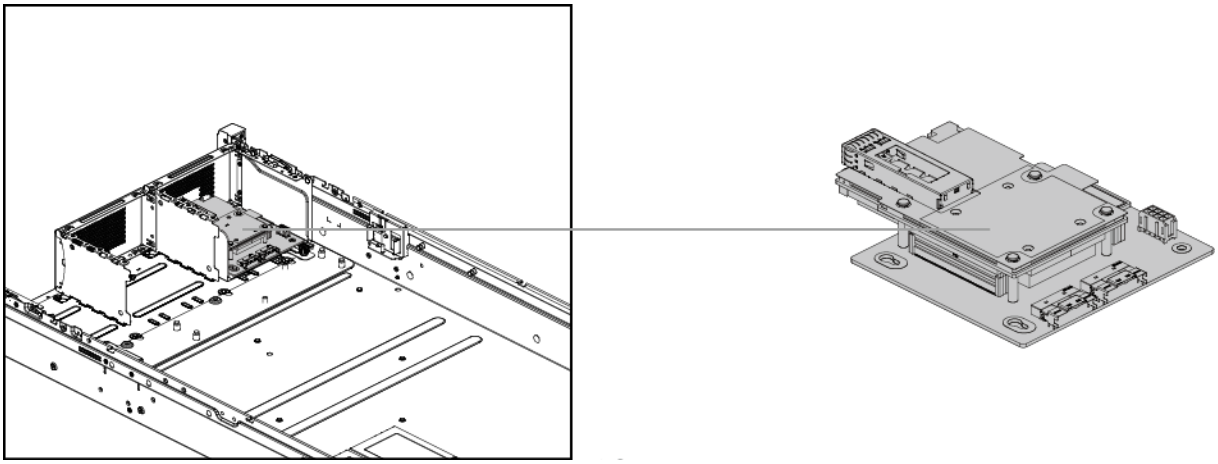


Figure 2-34 OCP Card Location

Reminder

Before you remove or install the OCP card, please follow the steps below:

Step 1: *Make sure the server is not turned on or connected to the AC power. To power off the server, see "2.1.1 Power Off".*

Step 2: *Remove the rear chassis cover. To remove the rear chassis cover, see"2.2 Rear Chassis Cover".*

Step 3: *Remove the front top cover. To remove the front top cover, see "2.3 Front Top Cover".*

Step 4: *Disconnect all the necessary cables.*

2.14.1 To remove the OCP card

❶ Unscrew the OCP card.

❷ Remove the OCP card from the chassis.

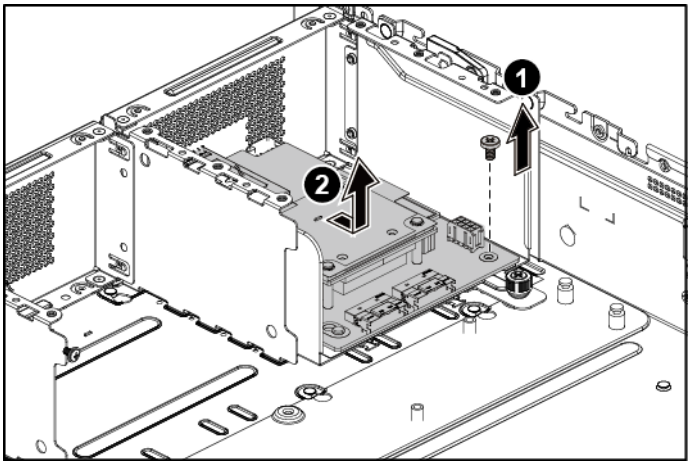


Figure 2-35 Removing the OCP Card

2.14.2 To install the OCP card

Reverse the steps above to install the OCP card.

2.15 Expansion Cards

The locations of expansion card assemblies on the server are shown below:

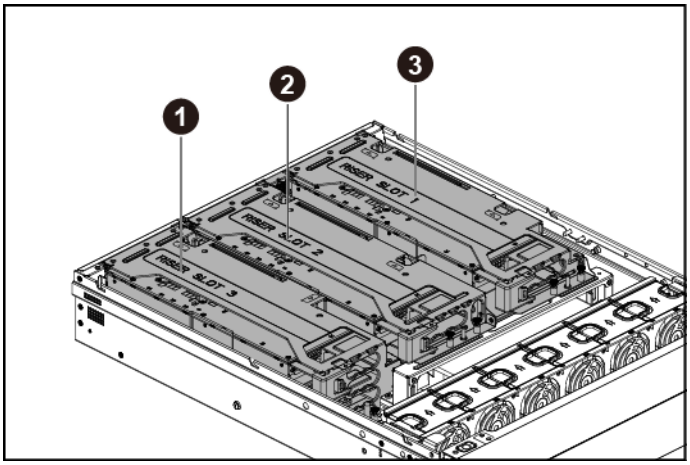


Figure 2-36 Expansion Card Assembly Locations

Reminder

Before you remove or install the expansion cards, please follow the steps below:

Step 1: *Make sure the server is not turned on or connected to the AC power. To power off the server, see "2.1.1 Power Off".*

Step 2: *Remove the rear chassis cover. To remove the rear chassis cover, see"2.2 Rear Chassis Cover".*

2.15.1 To remove the expansion card

❶ Unscrew the expansion card assembly.
❷ Lift the expansion card assembly out of the chassis.

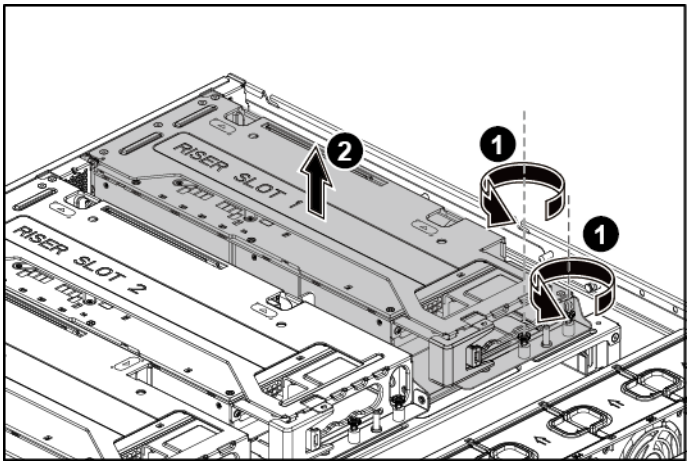


Figure 2-37 Removing the Expansion Card Assembly

❸ Push the locking clip along the direction of the arrow to release the clip.

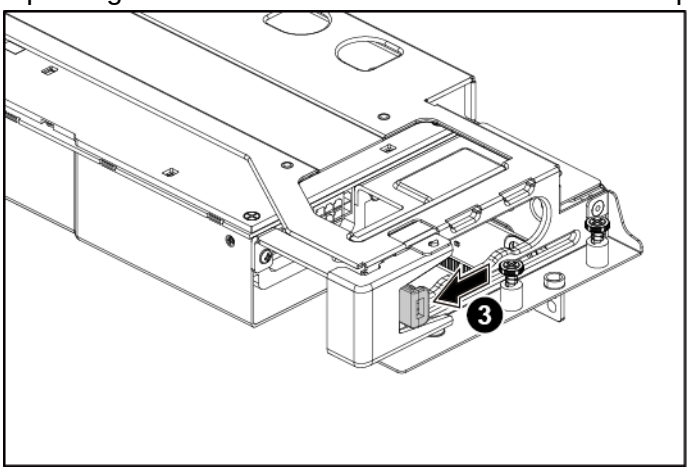


Figure 2-38 Releasing the Clip

❹ Rotate the clip to release the GPU.
❺ Unscrew the GPU.
❻ Remove the GPU.
❼ Install the slot covers.

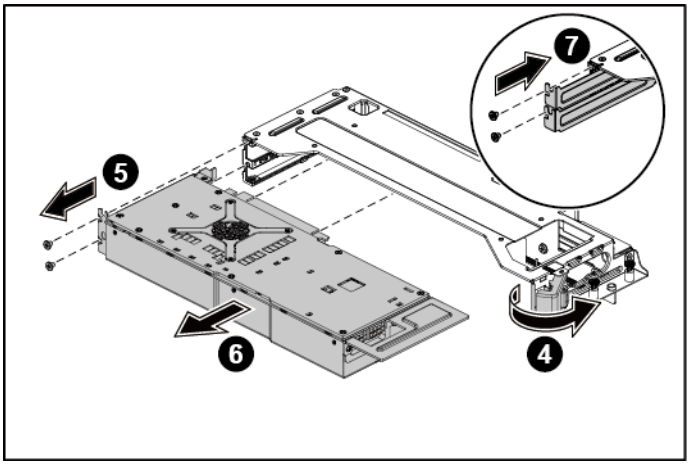


Figure 2-39 Removing the GPU

❽ Remove the screw that secures the riser card.
❾ Remove the riser card.

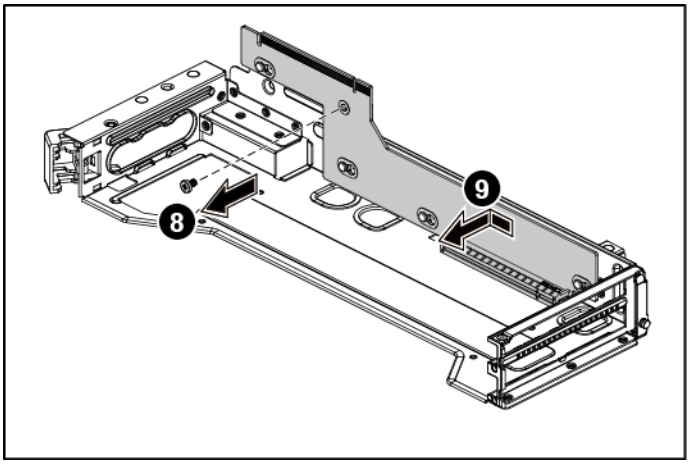


Figure 2-40 Removing the Riser Card

2.15.2 To install the expansion card

Reverse the steps above to install the expansion card.

2.16 Fan Duct

The location of fan duct on the server is shown below:

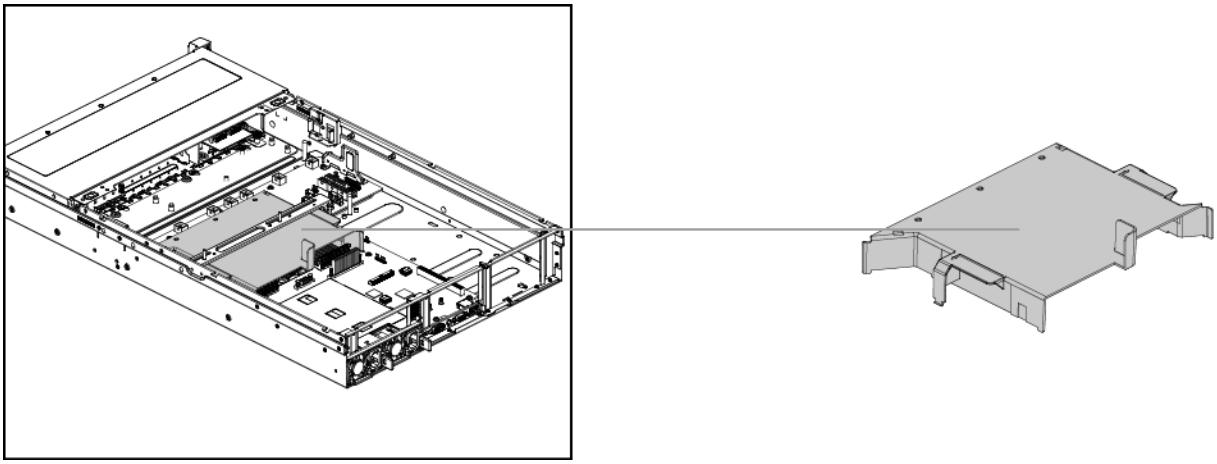


Figure 2-41 Fan Duct Location

Make sure that the fan duct on the server is installed in place to keep proper cooling.

Reminder

Before you remove or install the fan duct, please follow the steps below:

Step 1: *Make sure the server is not turned on or connected to the AC power. To power off the server, see "2.1.1 Power Off".*

Step 2: *Remove the rear chassis cover. To remove the rear chassis cover, see"2.2 Rear Chassis Cover".*

Step 3: *Remove the stiffener. To remove the stiffener see "2.5 Stiffener".*

2.16.1 To remove the fan duct

Lift the fan duct out of the chassis.

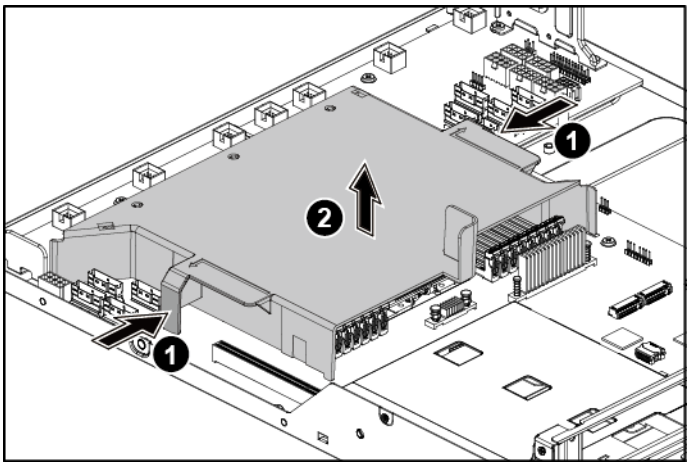


Figure 2-42 Removing the Fan Duct

2.16.2 To install the fan duct

Reverse the steps above to install the fan duct.

Chapter 3
Connectors

Backplane Connectors
OCP Card Connectors

3 Connectors

3.1 Backplane Connectors

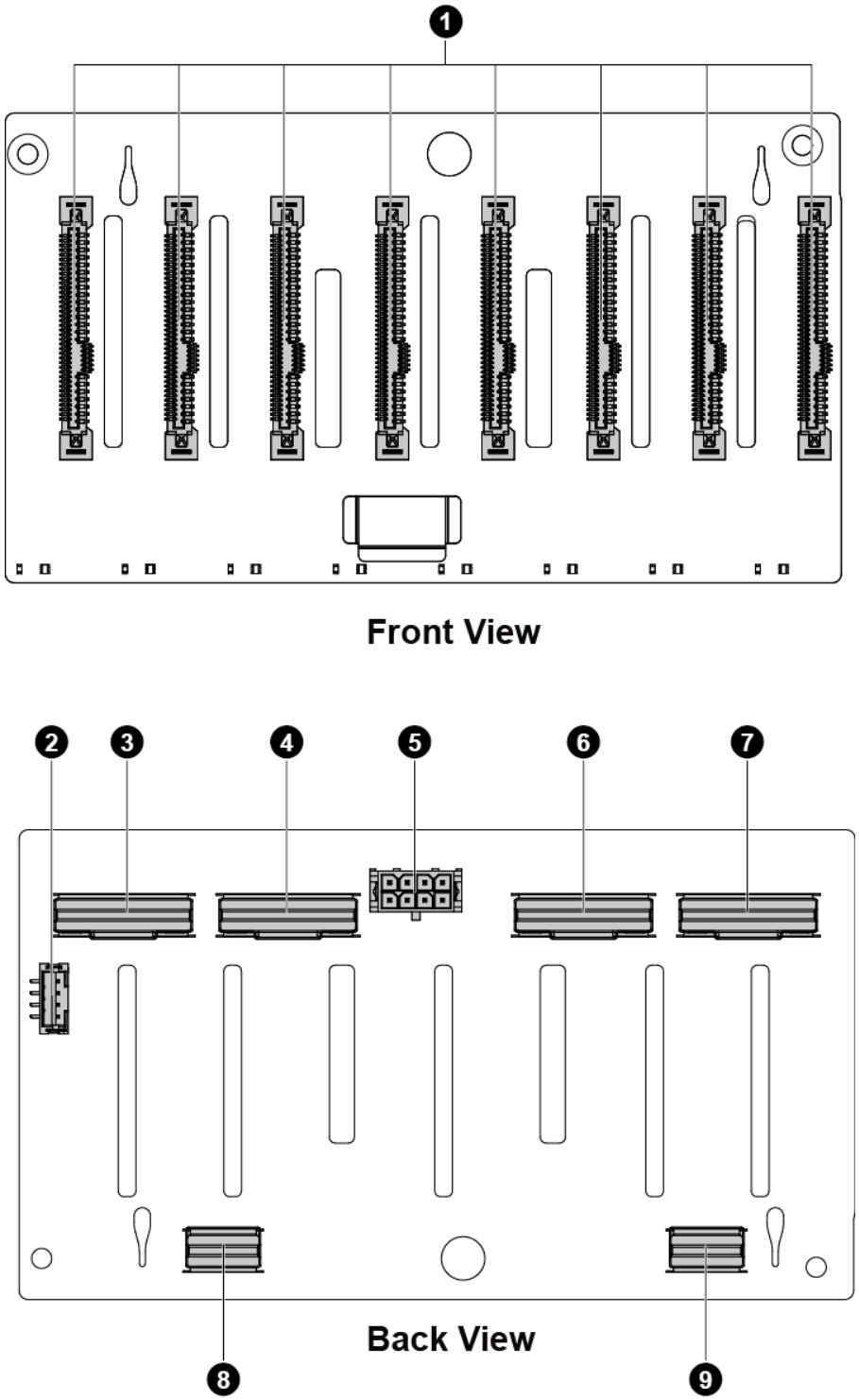


Figure 3-1 8x2.5“ HDDs Backplane

1	SATA HDD Connectors 0-7	6	Slimline Connector 2
2	I^2C Connector	7	Slimline Connector 1
3	Slimline Connector 4	8	Backplane SATA Connectors 2
4	Slimline Connector 3	9	Backplane SATA Connectors 1
5	Backplane Power Connector		

3.2 OCP Card Connectors

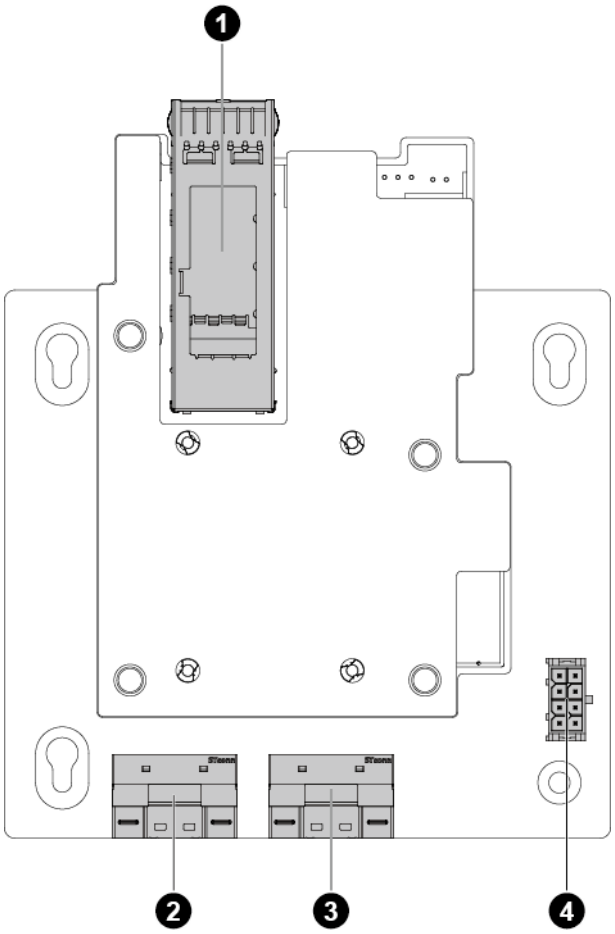


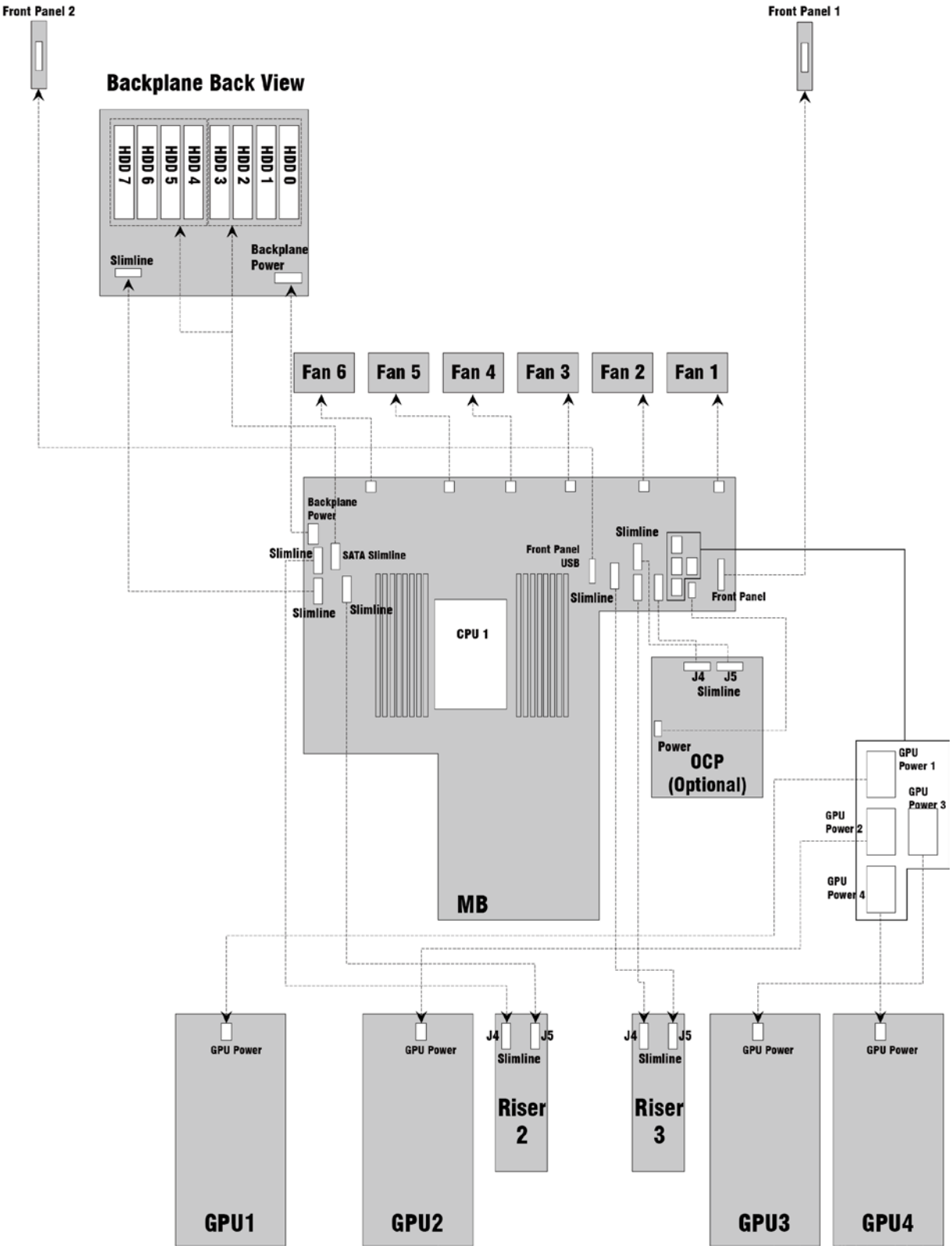
Figure 3-2 OCP Card

1	QSFP Ports	3	Slimline Connector 1
2	Slimline Connector 2	4	NCSI Connector

Chapter 4

Cable Routing

4 Cable Routing



Appendix 1

China RoHS Regulations

Taiwan BSMI

Electromagnetic Emissions Notices

Appendix 1 Hazardous Substances Free Regulations and Electromagnetic Emissions Notices

China RoHS Regulations

产品中有害物质的名称及含量状态说明表

部件名称	有毒有害物质或元素					
	铅（Pb）	汞（Hg）	镉（Cd）	六价铬（Cr(VI)）	多溴联苯（PBB）	多溴二苯醚（PBDE）
机箱/ 挡板	×	○	○	○	○	○
机械部件（风扇、散热器、马达等）	×	○	○	○	○	○
印刷电路部件	×	○	○	○	○	○
电缆/ 电线/ 连接器	×	○	○	○	○	○
硬盘驱动器	×	○	○	○	○	○
介质读取/ 存储设备	×	○	○	○	○	○
电源设备/ 电源适配器	×	○	○	○	○	○
电源线	×	○	○	○	○	○
完整机架/ 导轨产品	×	○	○	○	○	○

○：表示该有毒有害物质在该部件所有均质材料中的含量均在 GB/T 26572 标准规定的限量要求以下。

×：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 GB/T 26572 标准规定的限量要求。

注意：

1. 本表显示英业达股份有限公司供应的本型号产品可能包含这些物质，这些有毒有害物质或元素的部件皆因全球技术发展水平限制而无法实现有毒有害物质或元素的替代，但这些信息可能随着技术发展而不断更新。
2. 根据型号的不同可能不全含有以上的所有部件，请以实际购买机型为准。
3. 本表中部件定义的解释权归属英业达股份有限公司。

右图为本型号产品的环保使用期限标志，某些可更换的零部件会有一个不同的环保使用期（例如：电池的环保使用期限为五年）此环保使用期限只适用于产品手册中所规定的条件下工作。

Figure I China RoHS Regulations

Taiwan BSMI

限用物質標示聲明書						
設備名稱：伺服器 Equipment name			型號(型式)：P47 Type designation (Type)			
單元	限用物質及其化學符號					
	鉛	汞 (Hg)	鎘 (Cd)	六價鉻 (Cr^{+6})	多溴聯苯 (PBB)	多溴二苯醚 (PBDE)
內外殼	—	○	○	○	○	○
電路板	—	○	○	○	○	○
主機板	—	○	○	○	○	○
記憶卡	—	○	○	○	○	○
電源供應器	—	○	○	○	○	○
存取裝置 (HDD、SSD)	—	○	○	○	○	○
散熱模組（主機風扇、CPU風扇）	—	○	○	○	○	○
配件（傳輸線、網路線）	—	○	○	○	○	○
其他固定組件（螺絲、檔板）	—	○	○	○	○	○
備考 1. “○”係指該項限用物質之百分比含量未超出百分比含量基準值。 備考 2. “—”係指該項限用物質為排除項目。						

Figure II　Taiwan BSMI

Electromagnetic Emissions Notices

Federal Communications Commission notice

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) this device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation.

Class A Equipment

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at personal expense.

Notices for Canada (Avis Canadien)

Class A Equipment

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations. CAN ICES-3(A)/NMB-3(A) Cet appareil numérique de la class A respecte toutes les exigences du Règlement sur le materiel brouilleur du Canada.

Notices for China

Class A Equipment

声明
此为 A 级产品，在生活环境中，该产品可能会造成无线电干扰。在这种情况下，可能需要用户对其干扰采取可行的措施。

Notices for European Union

European Union Regulatory Notice

Products bearing the CE marking comply with applicable EU Directives:

Compliance with such directives is assessed using applicable European Harmonized Standards.

Notices for Japan

VCCI Notice

Class A EMI Warning Message

VCCI マークが付いていない場合には、次の点にご注意下さい。

この装置は、クラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者は適切な対策を講ずるよう要求されることがあります。

VCCI-A

Power Cord Statement

製品には、同梱された電源コードをお使い下さい。
同梱された電源コードは、他の製品では使用出来ません。

Notices for Korea

Class A EMI Warning Message

A급 기기 (업무용 방송통신기기)	이 기기는 업무용(A급)으로 전자파적합등록을 한 기기이오니 판매자 또는 사용자는 이 점을 주의하시기 바라며, 가정 외의 지역에서 사용하는 것을 목적으로 합니다.

Notices for Taiwan

BSMI Notices

Class A EMI Warning Message

警告使用者：

此為甲類資訊技術設備，於居住環境中使用時，可能會造成射頻擾動，

在此種情況下，使用者會被要求採取某些適當的對策。

Notices for Russia

Class A EMI Warning Message

ВНИМАНИЕ!
Настоящее изделие относится к оборудованию класса А. При использовании в бытовой обстановке это оборудование может нарушать функционирование других технических средств в результате создаваемых индустриальных радиопомех. В этом случае от пользователя может потребоваться принятие адекватных мер.

Appendix 2

BIOS SPEC

BIOS Setup User Manual

K800QG4

rev. 0.01

Mar., 2018

Table of Contents

1 Main 1
2 Advanced 2
3 Platform 8
4 Socket 10
5 BMC 19
6 Security 20
7 Boot 21
8 Save & Exit 22

1 Main

System brief overview.

- Project Version
  The current version of BIOS.
- Build Date and Time
  The date that BIOS image was created.
- Platform
  Basic info of sytem platform.
- Processor
  Basic info of system Processor.
- Total Memory
  Total Memory size.
- System Date
  Set the Date. Use Tab to switch between Date elements.
  Default Ranges:
  Year: 1998-9999
  Months: 1-12
  Days: dependent on month
- System Time
  Set the Time. Use Tab to switch between Time elements.

2 Advanced

Advanced settings. Includes the driver interface, serail port setting, TPM, CSM, NVME configuration and USB setting.

▶ iSCSI Configuration

Configure the iSCSI parameters.

- Add an Attempt
  Use this option to configure an iSCSI boot target.
- Delete Attempts
  Delete one or more attempts.
- Change Attempt Order
  Change Attempt Order.

▶ Driver Health

Driver Health status

▶ Trusted Computing

Trusted Computing Settings.

Note: Please remember to install TPM module in advance.

- Security Device Support
  Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
  - [Enable]*
  - [Disable]
- TPM State
  Enable/Disable Security Device. NOTE: Your Computer will reboot during restart in order to change State of the Device.
  - [Enable]*
  - [Disable]
- Pending operation

Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.

■ [None]*

■ [TPM Clear]

- Current Status Information
  Current Status Information.

- TPM Enabled Status
  Enabled Status of TPM.

- TPM Active Status
  Active Status of TPM.

- TPM Owner Status
  Owner Status of TPM.

- TPM20 Device Found
  TPM20 Device Found or not

▶ Serial Port Console Redirection

Serial Port Console Redirection configuration.

- Console Redirection
  Serial Port Console Redirection.
  ■ [Enable]*
  ■ [Disable]

Note: POST will not be full screen until this item is disabled.

▶ Console Redirection Settings

The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

- Terminal Type
  Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
  ■ [VT100]

- [VT100+]
- [VT-UTF8]
- [ANSI]*

- Bits per second

  Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
  - [9600]
  - [19200]
  - [57600]
  - [115200]*

- Data Bits

  Data Bits.
  - [7]
  - [8]*

- Parity

  A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
  - [None]*
  - [Even]
  - [Odd]
  - [Mark]
  - [Space]

- Stop Bits

  Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
  - [1]*
  - [2]

- Flow Control

  Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the

data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.

- [None]*
- [Hardware RTS/CTS]

- EMS

  Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.

  - [Enable]*
  - [Disable]

▶ PCI Subsystem Settings

PCI Settings Common for all Devices.

- SR-IOV Support

  If system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support.

  - [Enable]
  - [Disable]*

▶ Network Stack Configuration

Network Stack Settings

- Network Stack

  Enable/Disable UEFI Network Stack.

  - [Enable]
  - [Disable]*

- Ipv4 PXE Support

  Enable Ipv4 PXE Boot Support. If disabled IPV4 PXE boot option will not be created.

  - [Enable]*
  - [Disable]

- Ipv4 HTTP Support

  Enable Ipv4 HTTP Boot Support. If disabled IPV4 HTTP boot option will not be created.

  - [Enable]*
  - [Disable]

- Ipv6 PXE Support

Enable Ipv6 PXE Boot Support. If disabled IPV6 PXE boot option will not be created.

- [Enable]*
- [Disable]

- Ipv6 HTTP Support

  Enable Ipv6 HTTP Boot Support. If disabled IPV6 HTTP boot option will not be created.
  - [Enable]*
  - [Disable]

- PXE boot wait time

  Wait time to press ESC key to abort the PXE boot.
  - [0]*
  - ~
  - [5]

- Media detect count

  Number of times presence of media will be checked.
  - [1]*
  - ~
  - [50]

▶ CSM Configuration

CSM Configuration.

- CSM Support

  Enable/Disable CSM Support.
  - [Enable]*
  - [Disable]

- Boot option filter

  This option controls Legacy/UEFI ROMs priority.
  - [UEFI and Legacy]*
  - [Legacy only]
  - [UEFI only]

- Network

  Controls the execution of UEFI and Legacy PXE OpROM.
  - [UEFI]*
  - [Legacy]

- Storage

  Controls the execution of UEFI and Legacy Storage OpROM.

  - [UEFI]*
  - [Legacy]

- Video

  Controls the execution of UEFI and Legacy Video OpROM.

  - [UEFI]
  - [Legacy]*

> Note: BIOS would no't display info to monitor under legacy OS if you select UEFI mode.

▶ NVMe Configuration

NVMe status and configuration.

▶ USB Configuration

USB devices and configuration.

- USB Mass Storage Driver Support

  Enable or Disable USB mass storage driver support.

  - [Enable]*
  - [Disable]

3 Platform

Platform and PCH configuration options

▶ PCH Configuration

PCH Configuration.

- Restore AC Power Loss

  Provides the policy whether or not the system should boot once power returns after a power loss event.

  - [Power Off]
  - [Power On]
  - [Last State]*

▶ PCH SATA Configuration

PCH SATA(Serial Advanced Technology Transport) Configuration.

- SATA Controller

  Enable or Disable SATA Controller.

  - [Enable]*
  - [Disable]

- Configure SATA as

  This will configure SATA as RAID or AHCI.

  - [AHCI]*
  - [RAID]

▶ PCH sSATA Configuration

PCH sSATA(Server Serial Advanced Technology Transport) Configuration.

▶ Miscellaneous Configuration

Miscellaneous items configuration.

- Active Video

  Select active Video type.

  - [Auto]*
  - [On board device]
  - [PCIE Device]

Note: The priority of the external video card will be higher than on board device with "Auto" option.

- RTC Wake system from S4/S5
  RTC Wake system from S4/S5.
  - ■ [Disable]*
  - ■ [Enable]

▶ Server ME Configuration

Intel ME(Management Engine) Configuration.

- General ME Configuration
  Configure Server ME Technology Parameters.
- Oper. Firmware Version
  Version of operational firmware selected to run.
- Current State
  ME firmware Current State, bits [3:0] in MEFS1.
- Error Code
  ME firmware Error Code, bits [15:12] in MEFS1.
- Recovery Cause
  Server ME firmware recovery cause, bits [10:8] in MEFS2.

4 Socket

Socket and memory features configuration

▶ Processor Configuration

Processor status & configuration.

- Hyper-Threading

  Enables Hyper Threading (Software Method to Enable/Disable Logical Processor threads.

  - [Disable]
  - [Enable]*

- Enable Intel(R) TXT

  Enables Intel(R) Trusted Execution Technology.

  - [Disable]*
  - [Enable]

- VMX

  Enables the Vanderpool Technology, takes effect after reboot.

  - [Disable]
  - [Enable]*

- Enable SMX

  Enables Safer Mode Extensions.

  - [Disable]*
  - [Enable]

- Extended APIC

  Enable/disable extended APIC support.

  - [Disable]*
  - [Enable]

- Force x2APIC IDs

  Force use of > 8-bit APIC IDs.

  - [Disable]*
  - [Enable]

- AES-NI

Select Enable to use the Intel Advanced Encryption Standard (AES) New Instructions (NI) to ensure data security.

- [Disable]
- [Enable]*

▶ Common RefCode Configuration

Displays and provides option to change the Common RefCode Settings.

- Numa

  Enable or Disable Non uniform Memory Access (NUMA).

  - [Disable]
  - [Enable]*

▶ UPI Configuration

Displays and provides option to change the UPI Settings.

▶ UPI General Configuration

UPI General Configuration.

▶ UPI Status

UPI Status.

- Current UPI Link Frequency

  Intel® Ultra Path Interconnect (Intel® UPI) Link Frequency.

▶ Memory Configuration

Memory Configuration.

- Memory Frequency

  "Maximum Memory Frequency Selections in Mhz. Do not select Reserved.

  - [Auto]*
  - [1866]
  - [2133]
  - [2400]
  - [2666]

- Enable ADR

  Asynchronous DRAM Refresh (ADR) preserves key data in the battery-backed DRAM in the event of AC power supply failure.

  - [Disable]

- [Enable]*

- Erase-Arm NVDIMMs
  Enables/Disables Erasing and Arming NVDIMMs.

▶ Memory Topology

Displays memory topology with Dimm population information.

▶ Memory Map

Set memory mapping settings.

- Channel Interleaving
  Select Channel Interleaving setting.
  - [Auto]*
  - [1-way Interleave]
  - [2-way Interleave]
  - [3-way Interleave]

▶ Memory RAS Configuration

Displays and provides option to change the Memory Ras Settings.

- Static Virtual Lockstep Mode
  Enable Static Virtual Lockstep mode.
  - [Disable]*
  - [Enable]

- Mirror mode
  Mirror Mode will set entire 1LM/2LM memory in system to be mirrored, consequently reducing the memory capacity by half. Mirror Enable will disable XPT Prefetch.
  - [Disable]*
  - [Mirror Mode 1LM]
  - [Mirror Mode 2LM]

- Memory Rank Sparing
  Some memory ranks in each DDR channel can be set aside as spare memory during memory initialization. When a DDR rank's reliability is at doubt, the contents are migrated to spare ranks and the failing rank is turned off. In this model, part of system memory is sacrificed. For example:

If 4G QR memory DIMMs are populated, then in Single Rank Sparing 12.5% (1G / 8G in each DDR Channel) of memory is sacrificed as spare.

Rank Sparing Rules:
1. There must be at least 2 ranks in a DDR channel to support rank sparing
2. Up to 2 of ranks in a DDR channel can be spared
3. Spare Rank must be same or bigger in size than any rank in the DDR Channel
4. Prioritize Rank Sparing over Device tagging

■ [Disable]*
■ [Enable]

- Correctable Error Threshold
  Correctable Error Threshold (1 - 32767) used for sparing, tagging, and leaky bucket.
  ■ [0]
  ~
  ■ [0x7FFF]*

- SDDC Plus One
  In SDDC Plus One mode, BIOS copies the entire rank to the ECC DRAM device, once it is in SDDC plus1 mode, there is no error correction for the rank, it is on error detection mode only.
  ■ [Disable]*
  ■ [Enable]

- SDDC
  Enable/Disable SDDC(single-device data correction).
  ■ [Disable]*
  ■ [Enable]

- ADDDC Sparing
  ADDDC(Adaptive Double Device Data Correction) is an improved implementation of Legacy DDDC, the memory channels are not in lockstep mode from boot time and hence improved performance. Like the legacy DDDC implementation, the first device failure is tolerated using a device sparing flow to map out the bad device, it uses X4 SDDC to tolerate the second device failure. ADDDC can operate at the bank granularity.
  ■ [Disable]*

■ [Enable]

● Patrol Scrub

Patrol scrubbing is accomplished using an engine that generates requests to memory addresses in a stride. Usually, the engine is programmed with a frequency. The engine will generate a memory request at the pre-programmed frequency, and the scrubbing flow corrects the error, if any. Scrub interval has moved from MC (HSX) to PCU (Skylake) in System address mode as well as in legacy mode. Scrub interval is programmed using the P-Code mail box command MAILBOX_BIOS_CMD_MC_PATROL_SCRUB_INTERVAL passing the scrub interval and mc number.

■ [Disable]

■ [Enable]*

● Patrol Scrub Interval

Selects the number of hours (1-24) required to complete full scrub. A value of zero means auto!

■ [0]

~

■ [24]*

▶ NGN Configuration

Displays and provides option to change the NGN settings

▶ NGNVM DIMM Secure Erase Unit

Erases the persistent memory region of the selected DIMMs.

▶ IIO Configuration

IIO General Configuration.

▶ Socket0 Configuration

Configuration for 1st socket.

▶ Socket 0 PcieBr00D00F0 - Port 0/DMI

DMI(Direct Media Interface) port satus.

● PCI-E Port Link Status

DMI link current status.

- PCI-E Port Link Max
  DMI max width.

- PCI-E Port Link Speed
  DMI link current speed.

▶ Socket 0 PcieBr1D00F0 - Port 1A

PCIE port 1A satus.

- PCI-E Port
  Enable/Disable the PCIE port.
  - [Auto]*
  - [Disable]
  - [Enable]

- Link Speed
  PCIE Link speed forceing selection.
  - [Auto]*
  - [Gen 1 (2.5GT/s)
  - [Gen 2 (5 GT/s)
  - [Gen 3 (8 GT/s)

- PCI-E Port Link Status
  PCIE link current status.

- PCI-E Port Link Max
  PCIE max width.

- PCI-E Port Link Speed
  PCIE link current speed.

▶ Socket1 Configuration

Configuration for 2nd socket.

▶ IOAT Configuration

I/O Acceleration Technology (I/OAT)
Server consolidation requires large numbers of virtual machines (VMs) per physical server. Intel I/OAT helps ensure that the resulting data traffic doesn't overwhelm server I/O.

Throughput: Improves CPU-network interface integration for better memory-copy performance
Scalability: Increases control over interrupt processing, including prioritization and resource allocation
Efficiency: Provides an alternative to interrupt and system-to-user memory copy operations for each packet

▶ Sck0 IOAT Config

Sck0 IOAT Configuration.

- DCA
  DCA Enable/Disable for this specific socket.
  - [Disable]*
  - [Enable]

- DMA
  Select DMA(Direct memory access) Enable/Disable for each CB device.
  - [Disable]
  - [Enable]*

- No Snoop
  No Snoop Enable/Disable for each CB device.
  - [Disable]*
  - [Enable]

▶ Intel® VT for Directed I/O (VT-d)

Intel® VT for Directed I/O (VT-d) Configuration.

- Intel®VT for Directed I/O (VT-d)
  Enable/Disable Intel® Virtualization Technology for Directed I/O (VT-d) by reporting the I/O device assignment to VMM through DMAR ACPI Tables.
  - [Enable]
  - [Disable]*

▶ Intel® VMD technology

Intel® VMD for Volume Management Device Configuration menu.

- Intel® VMD technology

Volume Management Device (VMD) - An integrated endpoint device that can take control of PCI hierarchies to allow for the aggregation of devices such as PCIe SSD into a RAID array.

▶ Intel® VMD for Volume Management Device on Socket 0

Intel® VMD for Volume Management Device on 1st socket

- Intel® VMD for Volume Management Device for PStack0
  Enable/Disable Intel® Volume Management Device Technology in this Stack.
  - [Disable]*
  - [Enable]

▶ VMD for Volume Management Device on Socket 1

Intel® VMD for Volume Management Device on 2nd socket

▶ Advanced Power Management Configuration

Displays and provides option to change the Power Management Settings.

▶ CPU P State Control

P State Control Configuration Sub Menu, include Turbo, XE and etc.

- SpeedStep (Pstates)
  Enable/Disable EIST (P-States)
  - [Disable]
  - [Enable]*

- EIST PSD Function
  Choose HW_ALL/SW_ALL/SW_ANY in _PSD return
  - [HW_ALL]*
  - [SW_ALL]
  - [SW_ANY]

- Energy Efficient Turbo
  Energy Efficient Turbo Disable, MSR 0x1FC [19]
  - [Enable]*
  - [Disable]

- Turbo Mode
  Enable/Disable processor Turbo Mode (requires EMTTM enabled too).

- [Disable]
- [Enable]*

▶ CPU C State Control

CPU C State setting.

- CPU C6 report

  Enable/Disable CPU C6(ACPI C3) report to OS.

  - [Disable]
  - [Enable]
  - [Auto]*

- Enhanced Halt State (C1E)

  Core C1E auto promotion Control. Takes effect after reboot.

  - [Disable]
  - [Enable]*

▶ Package C State Control

Set the limit on the C-State package register.

- Package C State

  Package C State limit.

  - [C0/C1 state]
  - [C2 state]
  - [C6(non Retention) state]
  - [C6(Retention) state]
  - [No Limit]
  - [Auto]*

▶ Memory Power & Thermal Configuration

Displays and provides option to change the Memory Settings.

5 BMC

Server management configuration.(Base Management Controller)

- FRB-2 Timer

  Enable or Disable FRB-2 timer(POST timer)

  - [Enable]*
  - [Disable]

- FRB-2 Timer Policy

  Configure how the system should respond if the FRB-2 Timer expires. Not available if FRB-2 Timer is disabled.

  - [Do Nothing]*
  - [Reset]
  - [Power Down]
  - [Power Cycle]

▶ View FRU information

View FRU information

▶ BMC network configuration

Configure BMC network parameters

- Configuration Address source

  Select to configure LAN channel parameters statically or dynamically(by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase.

  - [Unspecified]
  - [Static]
  - [DynamicBmcDhcp]*
  - [DynamicBMCNonDhcp]

- IPV6 Support

  Enable or Disable LAN1 IPV6 Support.

  - [Enable]*
  - [Disable]

6 Security

Admin passwaord & user password setting for BIOS boot or enter setup.

- Administrator Password
  Set Administrator Password.
- User Password
  Set User Password.

7 Boot

System boot settings & boot Priorities.

- Bootup NumLock State

  Select the keyboard NumLock state.

  - [on]*
  - [off]

- Quiet Boot

  Enables or disables Quiet Boot option.

  - [Disable]
  - [Enable]*

- Boot Option Priorities

  Sets the system boot order.

- USB Devices BBS Priorities

  Set the order of the legacy devices in this group.

8 Save & Exit

Save & exit options.

- Save Changes and Exit
  Exit system setup after saving the changes.
- Discard Changes and Exit
  Exit system setup without saving any changes.
- Save Changes and Reset
  Reset the system after saving the changes.
- Discard Changes and Reset
  Reset system setup without saving any changes.
- Save Changes
  Save changes.
- Discard Changes
  Discard changes
- Restore Defaults
  Restore/Load Default values for all the setup options.
- Save as User Defaults
  Save the changes done so far as User Defaults.
- Restore User Defaults
  Restore the User Defaults to all the setup options.
- Boot Override
  Force Boot device this time.

Appendix 3

BMC SPEC

K800G4 - BMC Specification

June 22th, 2018

Table of Contents

1. IPMI Introduction 4
2. Overview of BMC 4
2.1 Thermal Sensor Allocation 4
2.2 BMC Self Test Behaviors 5
3. BMC Watchdog 5
3.1 IPMI Standard Watchdog 5
3.2 Automatic System Recovery 5
3.3 Watchdog Event Logging 6
3.4 FRB2 Timeout Detection 6
3.5 Started From System Reset 6
3.6 Started From System Warm Reboot 6
3.7 When FRB2 Timeout Happened 6
3.8 Watchdog Timer 6
4. LED Indicators 7
5. The Concept of Message Channel 7
5.1 Maximum IPMI Message Size 7
6. LAN 8
6.1. The LAN-Related Information 8
6.2. Default User Account 8
6.3. Default LAN Channel Configuration 8
7. System Event Log (SEL) 9
7.1. Time Synchronization 9
7.2. The Behavior when SEL is full. 9
8. Serial Interface 10
8.1. Serial Over LAN (SOL) 10
8.2. SOL Information 10
8.3. SOL Configuration 10
8.4. The Behavior of SOL 10
9. RMCP(IPMI v1.5)/RMCP+(IPMI v2.0) and Payload Support 11
9.1. Payload Type List 11
9.2. RMCP Payloads 11
9.3. RMCP+ Payloads 11
9.4. Cipher Suite of RMCP+ 11
10. Remote KVM 12
10.1. KVM over IP 12
10.2. Browser Support 12
10.3. Screen Resolution and Color Depth 12
10.4. Full Screen and Window Mode 12
10.5. Simultaneous Console Users 12
10.6. Launch KVM 12
11. Sensors Configurations 14

11.1. Full Sensor Records 13
11.2. Automatic CPU Thresholds (for Intel Platform only) 23
12. Supported Standard IPMI Commands 24
12.1. IPMI Global Commands 24
12.2. BMC Watchdog Timer Commands 24
12.3. BMC Device and Messaging Commands 24
12.4. Chassis Device Commands 25
12.5. Event Commands 25
12.6. PEF and Alerting Commands 26
12.7. Sensor Device Commands 26
12.8. FRU Device Commands 26
12.9. SDR Device Commands 26
12.10. SEL Device Commands 27
12.11. LAN Device Commands 27
12.12. Serial/Modem Device Commands 27
12.13. Command Forwarding Commands 27
12.14. Bridge Management Commands (ICMB) 27
12.15. Discovery Commands (ICMB) 28
12.16. Bridging Commands (ICMB)[8] 28
12.17. Event Commands (ICMB) [8] 28
12.18. OEM Commands for Bridge NetFn 28
12.19. Other Bridge Commands 28
13. BMC Booting 29
13.1. Redundant Firmware Image 29
13.2. Firmware Integrity Check 29
13.3. Boot Time 29
13.4. Boot Process 29

1. IPMI Introduction

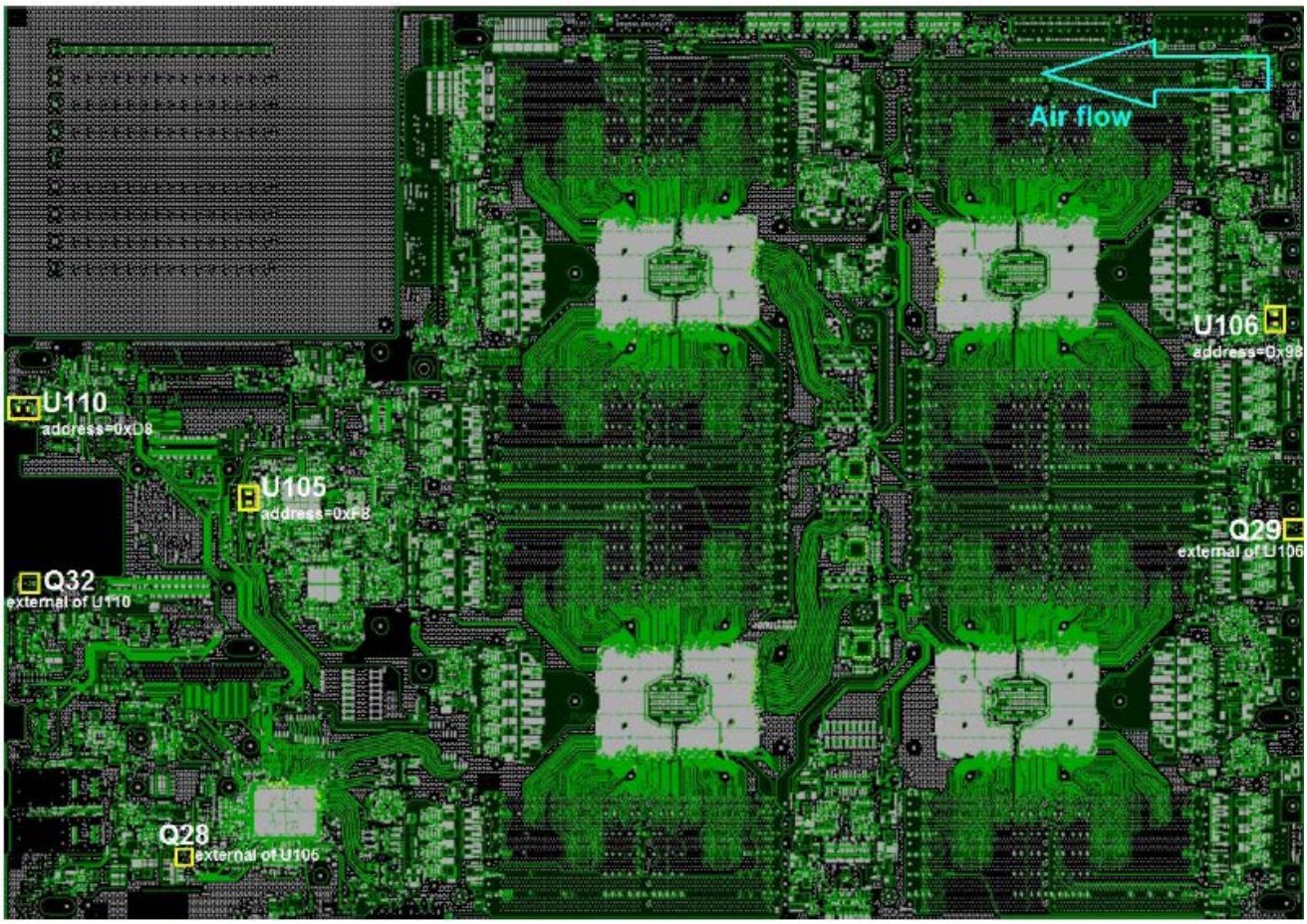
The IPMI is an abbreviation of Intelligent Platform Management Interface. This industrial standard is supported by INTEL, Hewlett-Packard, NEC, and Dell. Following this specification, we are able to monitor the system health of the server computer, such as fan speed, system and CPU temperature, voltage regulation, watchdog timer, power supply working condition.., etc. If an abnormal status was detected, it will be logged into the non-volatile memory device, preserved for later examination.

The key component behind the IPMI-based system is BMC, Baseboard Management Controller. It is the intelligence of the IPMI. BMC is like a sub-system resides on the system main board. It can keep monitoring the system status even at power off status. If necessary, it is possible for the BMC to reboot the system. BMC is connected to the various sensors via IPMB (Intelligent Platform Management Bus). IPMB is essentially a subset of I2C bus. System software could communicate with the BMC via KCS interface (Keyboard Controller Style). The detailed information of KCS will be explained in the following sections.

In this product, the implementation meets the specification of IPMI v2.0. This document defines the specification of BMC implementation, especially some system-specific features.

2. Overview of BMC

2.1 Thermal Sensor Allocation



2.2 BMC Self Test Behaviors

BMC do the self-test to check its health in boot time, runtime and IPMI Main process restarted. The following is the self-test item list.

- Check SDR
- Check SEL
- Check CRC

BMC would check those statuses at BMC runtime, while initial/write/delete/read SDR/SEL failed, the error bit would be set accordingly and user can retrieve the status by “Get Self Test Results Command”. BIOS would issue the ‘Get Self Test Results Command’ to get the BMC self-test results every time system power up(the result will show on BIOS setup menu), if the SEL-test failed, BMC would create a SEL for self-test failure, the error code (Get Self Test Results Command Response data Byte 2、3). The event would not be stored in SEL because of SEL function abnormally.

Behavior	Byte	Data Filed
Request	1	Completion Code-
Response	1	55h = No error. All Self Tests Passed. 56h = Self Test function not implemented in this controller. 57h = Corrupted or inaccessible data or devices 58h = Fatal hardware error (system should consider BMC inoperative). This will indicate that the controller hardware (including associated devices such as sensor hardware or RAM) may need to be repaired or replaced. FFh = reserved. all other: Device-specific ‘internal’ failure. Refer to the particular device’s specification for definition.
	2	For byte 2 = 55h, 56h, FFh: 00h For byte 2 = 58h, all other: Device-specific For byte 2 = 57h: self-test error bit field. Note: returning 57h does not imply that all tests were run, just that a given test has failed. I.e. 1b means ‘failed’, 0b means ‘unknown’. [7] 1b = Cannot access SEL device [6] 1b = Cannot access SDR Repository [5] 1b = Cannot access BMC FRU device [4] 1b = IPMB signal lines do not respond [3] 1b = SDR Repository empty [2] 1b = Internal Use Area of BMC FRU corrupted [1] 1b = controller update ‘boot block’ firmware corrupted [0] 1b = controller operational firmware corrupted

3. BMC Watchdog

A watchdog timer (WDT) is a device that performs a specific operation after a certain period of time if something goes wrong with an electronic system and the system does not recover on its own. And both hardware WDT and IPMI standard WDT was implemented on this platform.

3.1 IPMI Standard Watchdog

The BMC implement the SMS ‘OS watchdog’ & BIOS FRB2 watchdog timers in order to allow host software check pointing and system recovery on a timeout. The watchdog timer would be disabled by default. Beside system recovery on timeout, it also supports a pre-timeout interrupt using the KCS non-communication messaging interrupt (SMS_ATN flag).

3.2 Automatic System Recovery

The BMC supports the watchdog related command defined in IPMI v2.0 Spec for BIOS/SMS. The SMS /BIOS can use these timer functions to support the automatic system recovery function. Note that one who acquired and activated the watchdog timer is responsible to reset the timer countdown. If the pre-defined interval expired, the configured timer actions will be executed. Also, the event of watchdog timeout will be logged into SEL for later examination. The timeout action list as below:

- Hard Reset
- Power Down
- Power Cycle

3.3 Watchdog Event Logging

Any BMC watchdog timer expired would result in a SEL event being generated to indicate the watchdog timer timeout occurred and which timer (BMC hardware, OS or FRB2) caused the timeout action.

3.4 FRB2 Timeout Detection

The FRB2 timer is implemented with IPMI Watchdog Timer. The BMC supports BMC Watchdog Timer Commands. The following is the behavior of FRB2 timer.

3.5 Started From System Reset

a. BIOS tell BMC to enable Watchdog Timer of FRB2. And BIOS continues the POST process. The Watchdog Timer of FRB2 is set to 480 sec (set by BIOS).

b. During the execution of POST, in some circumstances, BIOS is forced to stop the Watchdog Timer for FRB2 for a while. There are 2 cases the FRB2 timer could be paused by BIOS:
   - Upon enter BIOS Setup menu.
   - Option ROM initial, etc… (It can be customized to tune the initialed time.)

c. In order to prevent the Watchdog Timer for FRB2 from expiring, BIOS has to reset the watchdog countdown within appropriate time interval. Finally, BIOS executes its last POST task (INT 19h). Then BIOS has to disable the Watchdog Timer of FRB2.

3.6 Started From System Warm Reboot

No matter system cold reset or warm reset, it would be monitored by a BIOS initiated watchdog timer. Their behavior is similar to the above descriptions.

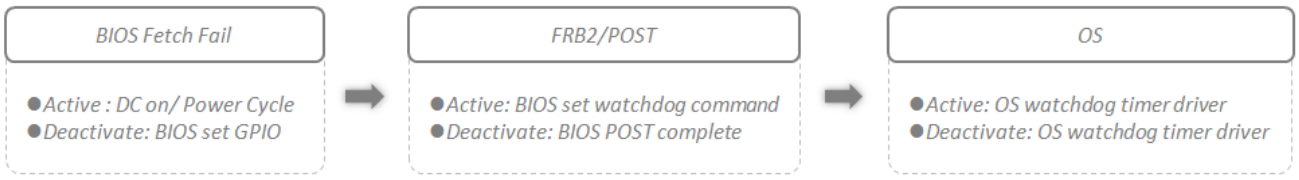
3.7 When FRB2 Timeout Happened

If the Timer expired from FRB2 over 3 times, BMC will “Power down” the system as the policy to avoid system “Hard Reset” again and again.

Sensor Type	Event/Reading Type	Sensor Specific Offset	Event
Watchdog2(0x23)	Sensor-specific(0x6F)	0x01	BIOS/FRB2 timeout generated hard reset
Event Data 1	**Event Data 2**	**Event Data 3**	
0xC1	[3:0]Timer use = 0x01 BIOS/FRB2	0xFF	

3.8 Watchdog Timer

BIOS code will be executed when CPU ready. So if BIOS wouldn’t tell BMC code is fetched in 20 seconds, it causes the watchdog timer expired. After this stage, BIOS needs to set FRB2 timer enable. After BIOS POST complete, BIOS also disable FRB2 timer. If user enables “OS load timer”, BIOS needs to enable “OS Load Timer” after FRB2.



4. LED Indicators

Name	Color	State	Before BMC Ready	BMC Ready	Position
System Health	--	On/Off	Control By CPLD	Sensor not all ready; BIOS Post not complete	Front Panel
	Green	On		System is Good. No Error	
	Red	On/Off		Critical voltage/temp; Any Fan fail; Any PSU not detect; Any HDD not detect	
UID	Blue	On	UID LED only is controlled by CPLD when BMC is not ready or boot fail.	UID is able to be controlled by BMC and UID button. Blink is only be controlled by BMC command.	Front Panel
		Off			
		Blink			
Heart Beat	Green	On	Heart Beat LED is On when AC On. After BMC ready, BMC will control Heart Beat LED blink when BMC is alive.		MB
		Blink (1Hz)			
Fan LED	Green	on	Fan good		Fan
	Red	off	Fan fail		

5. The Concept of Message Channel

In IPMI v2.0, there are the channels as KCS, IPMB, LAN and Serial/Modem…, etc. With the help of message channel, now BMC could accept requests from remote clients and send response messages back to other places far away. Because of security consideration, remote clients are required to login before sending IPMI commands. Users from System Interface and IPMB are regarded as local users. No user authentication is required for these two channels.

The following is a brief table of BMC supported channels. For detailed implementation of LAN and Serial/Modem channels, refer to their respective chapters of IPMI v2.0 Spec. Please note that the Serial/Modem channel is not supported in this implementation. The default system base address for an I/O mapped KCS SMS Interfaces is 0xCA2/0xCA3. The detail information refers the IPMI v2.0 Spec.

Channel NO.	Protocol	Medium	Authentication	Access
0x00	IPMB(0x01)	IPMB, I2C(0x01)	None	Always available
0x01	IPMB(0x01)	802.3 LAN (04h)	None/MD2/MD5/ Straight Password	Always available
0x0F	KCS(0x05)	System I/F (0Ch)	None	Always available

5.1 Maximum IPMI Message Size

The BMC provide up to 200 bytes (Not include Net function code、Command Code、Bus ID、Slave address、Read Count) IPMI message size for the KCS and private I2C buses. It would be reflected in the response to the IPMI Get system Interface Capabilities command.

6. LAN

6.1 The LAN-Related Information

LAN function	Description
DHCP IP	Support
LAN protocol	RMCP(V1.5)、RMCP+(V2.0) support
ARP	This function is implemented by BMC. (Default: Enable)
Enabled Authentications	Administrator[Password]
Session timeout	1800s(default) + 10s(tolerance)
Multi session	Support Max 15 sessions simultaneously
Anonymous Login	Not Support
LAN Alerting	Support SNMP Trap
User account	Support 10 user account including USER ID 1-10
Cipher Suite Entry	Support 3 entry, Cipher Suite IDs: 1, 2, 3

6.2 Default User Account

The BMC have no any constraints on user account such as password retention limits, password strength, etc. (follow IPMI spec)

User ID	User Name	Password	Payload Access	Privilege	Notes	Default state
1	NULL	NULL	-	CALLBACK	NULL User Name	Disabled
2	“admin”	“admin”	SOL	ADMINISTRATOR	Default administrator account	Enabled

6.3 Default LAN Channel Configuration

LAN parameter	Value	Notes
IP address	0.0.0.0	Non-routable default IP address
IP Source	DHCP	
Net Mask	255.255.255.0	
Default Gateway	192.168.0.1	
Gratuitous ARP Generation	Enabled	
Gratuitous ARP Interval	4 seconds	
ARP response	Enabled	
Access Privilege Limit	Administrator	
Enabled Authentications	Administrator [Password]	All other authentication disabled
MAC address	Factory configured	

7. System Event Log (SEL)

The BMC provides a centralized, non-volatile System Event Log, aka SEL. System Event Logs are special messages that are sent by management controllers when they detect significant or critical system management events. This includes messages for events such as temperature threshold exceeded', 'voltage threshold exceeded', 'power fault', and etc.

7.1 Time Synchronization

Time stamping is a key part of event logging and tracking. SEL timestamp need to be set through BIOS or System Management Software. There are 3 scenarios that BMC would synchronize its Real Time clock (RTC) with the host system:

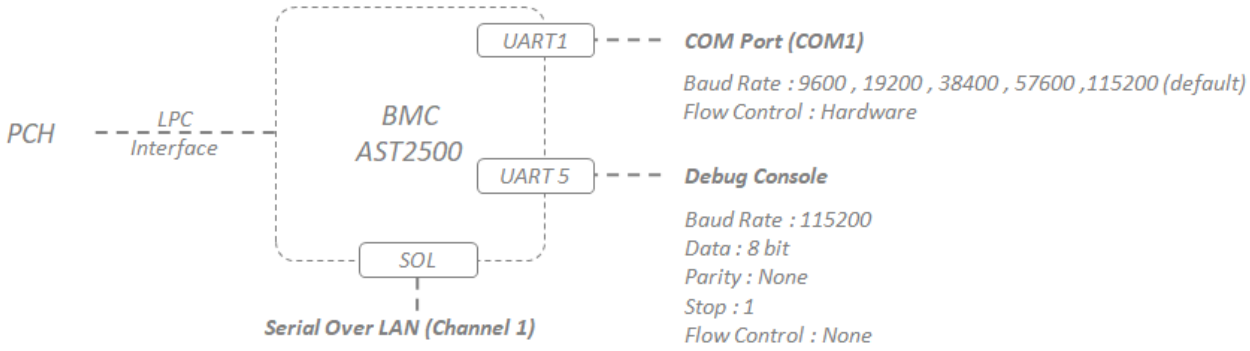
a. During system Power-on Self Test (POST), BIOS would wait BMC function ready (approximate 120 sec.), then send the Set SEL Time command with the current system time to sync RTC timer.
b. In runtime, on every BMC reset, BMC will assert GPIO to generate SMI to BIOS, then BIOS would send the Set SEL Time command with the current system time to sync RTC timer.
c. The BMC would automatically sync its RTC timer every 24 hours to maintain the tolerance within 3sec, via issue a SMI to BIOS.

Those events generated before the timestamp be set would show "Pre-Init Time-Stamp"as its timestamp, BMC will log SEL no matter the timestamp be set or not.

7.2 The Behavior when SEL is full.

- **Single Entry Delete**
  The *Delete SEL Entry* Command of IPMI is able to remove the individual records.
- **SEL Entry for SEL overflow**
  When SEL is about to fill, the last entry recorded would be a SEL entry stating the SEL has overflowed. This entry gives the system an indication that subsequent SEL entries were lost.
- **SEL Circle Log**
  When SEL is full, the system will record an "overflow" message and the oldest log is instead of a new one. And then it records an event for "SEL full".
- **SEL Clear**
  When all events are captured by SMS tool, SMS tool is able to clear SEL entry. After all events are cleaned, SEL agent will create a new event for this action.

8. Serial Interface



8.1 Serial Over LAN (SOL)

Serial over LAN provides a mechanism that enables the serial controller of a managed system to be redirected over an IPMI session over IP. This enables remote console applications to provide access to text-based interfaces for BIOS, utilities, operating systems, and applications while simultaneously providing access to IPMI platform management functions. SOL is implemented as a payload type under the new payload capability in RMCP+. This can be used to enable asynchronous serial-based OS and pre-OS communication over a connection to the BMC.

8.2 SOL Information

Item	Description
Channel#	0x01
Baud Rate	9600、19200、38400、57600、115200(default) BPS
Flow control	Hardware flow control
Payload port	623

8.3 SOL Configuration

LAN parameter	Value	Notes
SOL Enable	Disabled	Disable SOL payload type
SOL Authentications	Administrator	Administrator access over SOL
Non-Volatile Bit Rate	115200	115200 baud rate.
Volatile Bit Rate	115200	115200 baud rate.
Gratuitous ARP Interval	4 seconds	
ARP responses	Enabled	
Access Mode	Enabled	
Access Privilege Limit	Enabled	
Enabled Authentications	Administrator[Password]	All other Authentications disabled.
SOL Payload Access	Enabled	Enable SOL payload access.

8.4 The Behavior of SOL

The BMC is able to connect and switch UART port between COM Port 1 and SOL. If the SOL connection is abnormal, the watchdog of BMC would reset itself and return configuration (routing) to the default settings.

9. RMCP(IPMI v1.5)/RMCP+(IPMI v2.0) and Payload Support

"Payloads" are a capability specified for RMCP+ that enable an IPMI session to carry types of traffic that are in addition to IPMI Messages. In this project we support following payload type, Authentication Algorithm, Integrity Algorithm, and Confidentiality Algorithm. In IPMI v2.0 Spec, the RMCP+ session connection support one-key & two-key login option. This function also is implemented in this project. Following list the RMCP+ and payload characteristics in this project.

9.1 Payload Type List

Payload Type Number	Type	Major Format Version B[7:4]	Minor Format Version B[3:0]
0h	IPMI Message	0x01	0x00
1h	SOL (serial over LAN)	0x01	0x00

9.2 RMCP Payloads

Authentications	Status
OEM	Disable
Straight Password	Enable
MD5	Enable
MD2	Enable
None Authentication	Enable

9.3 RMCP+ Payloads

Algorithm		Admin	Operator	User	Callback	OEM
Authentication	None	O	X	O	O	X
	HMAC SHA1	O	O	O	O	X
	HMAC MD5	X	X	X	X	X
	HMAC SHA2	X	X	X	X	X
Integrity	None	O	O	O	O	X
	HMAC SHA1 96	O	O	O	O	X
	HMAC MD5 128	O	O	X	X	X
	MD5 128	X	X	X	X	X
	HMAC SHA2 128	X	X	X	X	X
Confidentiality	None	O	O	O	O	X
	AES CBC 128	O	O	O	O	X
	XRC4 128	X	X	X	X	X
	XRC4 40	X	X	X	X	X

9.4 Cipher Suite of RMCP+

ID	characteristics	Cipher Suite	Authentication Algorithm	Integrity Algorithm(s)	Confidentiality Algorithm(s)	Cipher Suite Priv. Max
1	S	01h, 00h, 00h	RAKP-HMAC-SHA1	None	None	Administrator
2	S,A	01h, 01h, 00h		HMAC-SHA1-96	None	Administrator
3	S,A,E	01h, 01h, 01h			AES-CBC-128	Administrator

Key:

S = authenticated session setup (correct role, username and password/key required to establish session)

A = authenticated payload data supported.

E = authentication and encrypted payload data supported

10. Remote KVM

The Keyboard, Video and Mouse (KVM) of server are able to redirect to remote system. Remote KVM provides greater control of hardware including access to power controls and monitoring functions through the Baseboard Management Controller (BMC). Remote KVM solutions provide more direct access to out-of-band system performance data and efficient integration with system-level monitoring information.

10.1 KVM over IP

Because Remote KVM solutions operate out-of-band of the system processor, they don't place undue burdens on the host processor. This also means that, although the Remote KVM resides in the server box, but it will not put extra loading to the host processor.

10.2 Browser Support

The embedded console client performs the KVM/IP functionality. This KVM client is based on HTML5 architecture. If browser of client is support HTML5, KVM could be used by user. Our suggest browsers as blow:

- Internet Explorer (IE) 11.0 or later version for Windows platforms.
- Firefox 34 or later version for all platforms
- Google Chrome 47 or later version

10.3 Screen Resolution and Color Depth

The client implements a dynamic selection of the different color depth and the screen resolution of the server. Following table shows the different combinations:

Resolution	Frequency	16-bit color	32-bit color
640x480	60	Yes	Yes
800x600	60	Yes	Yes
1024x768	60	Yes	Yes
1280x800	60	Yes	Yes
1280x1024	60	Yes	Yes
1440x900	60	Yes	Yes
1600x1200	60	Yes	Yes
1680x1050	60	Yes	Yes
1920x1080	60	Yes	Yes
1920x1200	60	Yes	Yes

The color depth can be chosen at any time while the console redirection is active. If the client (console side) has a lower screen resolution than that of the server side, then a scroll bar will be automatically displayed to view the entire screen. There is no fit-to-screen option for the screen resolution accommodation at the client side.

10.4 Full Screen and Window Mode

The console is capable of viewing the server side screen in both windowed and the full screen. In the full screen mode the display fills the entire screen area of the client. This provides a virtual presence feature of the server's screen.

10.5 Simultaneous Console Users

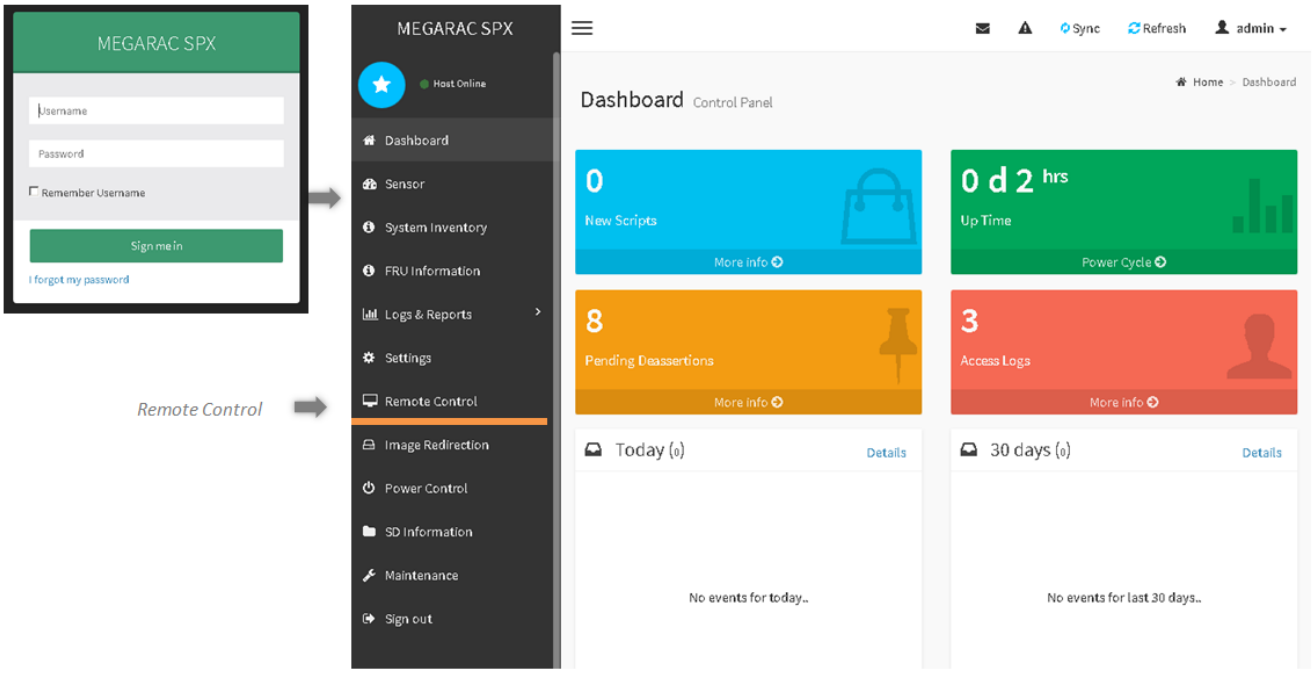
The KVM/IP console must provide up to three simultaneous users log-in. This feature should be configurable as 1 or 2 simultaneous console at a time. The first user gets the total control of the console including the keyboard/mouse. The others can only view the screen data or the activity.

10.6 Launch KVM

Step 1. Open one of the supported Browsers.

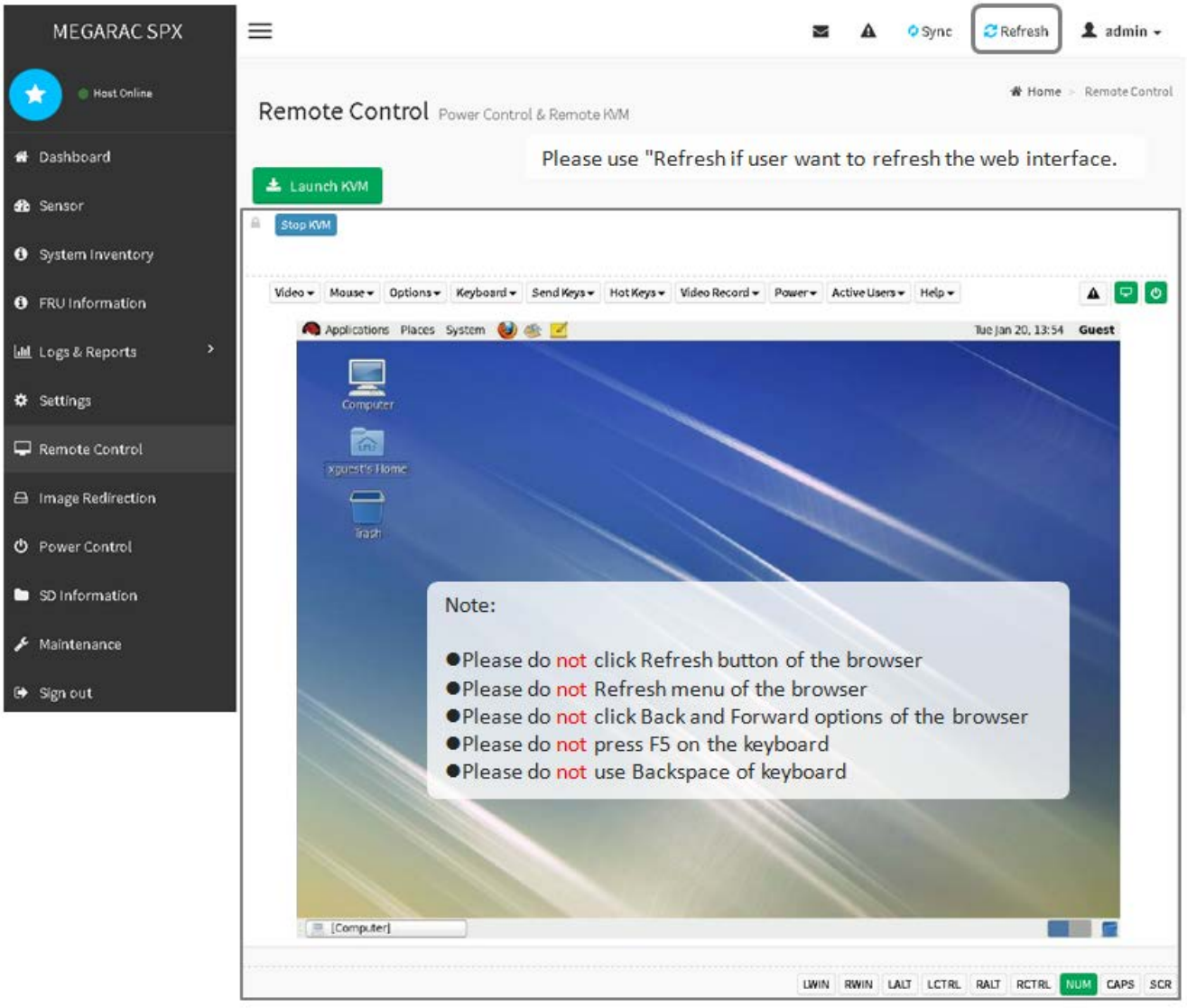
Step 2. Enter the IP as the web address.

Step 3. Enter the User name and password (IPMI user)to launch KVM.



Step 4. Select Remote Control from menu bar. Browser pops new window for KVM

Step 5. Click button Start KVM. If you want to terminate the KVM service, pleaser click "Stop KVM" button.



11. Sensors Configurations

11.1 Full Sensor Records

	1	2	3	4	5	6	7
Sensor Number	0x75	0x7A	0x7B	0x78	0x76	0x77	0x79
Sensor Name	AMBIENT_TEMP_01	AMBIENT_TEMP_02	AMBIENT_TEMP_03	OCP_TEMP_01	OCP_TEMP_02	OCP_TEMP_03	PCH_Temp_01
Sensor Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Event Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Entity ID	0x0C	0x07	0x07	0x07	0x07	0x07	0x07
Instance	0x01	0x02	0x02	0x02	0x01	0x01	0x01
Initialization	0x7F	0x7F	0x7F	0x7F	0x7F	0x7F	0x7F
Capabilities	0x68	0x68	0x68	0x68	0x68	0x68	0x68
AE/LTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
AE/LTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DE/UTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
DE/UTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DR/ST/RT Mask	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636
DR/ST/RT (BIT)	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/
LNR	0x00	0x00	0x00	0x00	0x00	0x00	0x00
LC	0x04	0x04	0x04	0x04	0x04	0x04	0x04
LNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UC	0x28	0x28	0x28	0x39	0x4B	0x39	0x39
UNR	0x2A	0x2A	0x2A	0x3C	0x4D	0x3C	0x3C
Resolution							

	8	9	10	11	12	13	14
Sensor Number	0x56	0x57	0x58	0x59	0x44	0x45	0x46
Sensor Name	CPU_ABS_TEMP_01	CPU_ABS_TEMP_02	CPU_ABS_TEMP_03	CPU_ABS_TEMP_04	CPU_TEMP_01	CPU_TEMP_02	CPU_TEMP_03
Sensor Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Event Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Entity ID	0x03	0x03	0x03	0x03	0x03	0x03	0x03
Instance	0x01	0x02	0x03	0x04	0x00	0x00	0x00
Initialization	0x7F	0x7F	0x7F	0x7F	0x7F	0x7F	0x7F
Capabilities	0x68	0x68	0x68	0x68	0x68	0x68	0x68
AE/LTR Mask	0x3005	0x3005	0x3005	0x3005	0x6A14	0x6A14	0x6A14
AE/LTR (BIT)	0/2/12/13/	0/2/12/13/	0/2/12/13/	0/2/12/13/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DE/UTR Mask	0x0005	0x0005	0x0005	0x0005	0x6A14	0x6A14	0x6A14
DE/UTR (BIT)	0/2/	0/2/	0/2/	0/2/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DR/ST/RT Mask	0x0303	0x0303	0x0303	0x0303	0x3636	0x3636	0x3636
DR/ST/RT (BIT)	0/1/8/9/	0/1/8/9/	0/1/8/9/	0/1/8/9/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/
LNR	0x00	0x00	0x00	0x00	0x00	0x00	0x00
LC	0x01	0x01	0x01	0x01	0x04	0x04	0x04
LNC	0x02	0x02	0x02	0x02	0x00	0x00	0x00
UNC	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x00
UC	0xFF	0xFF	0xFF	0xFF	0x61	0x61	0x61
UNR	0xFF	0xFF	0xFF	0xFF	0x66	0x66	0x66
Resolution							

- AM/LTR : Assertion Event Mask / Lower Threshold Reading Mask
- DEM/UTR : De-assertion Event Mask / Upper Threshold Reading Mask
- DE/UTR: Discrete Reading Mask / Settable Threshold Mask, Readable Threshold Mask

- LNR : Lower non-recoverable Threshold
- LC : Lower critical Threshold
- LNC : Lower non-critical Threshold
- UNC : Upper non-critical Threshold
- UC : Upper critical Threshold
- UNR : Upper non-recoverable Threshold

	15	16	17	18	19	20	21
Sensor Number	0x47	0x30	0x31	0x32	0x33	0x34	0x35
Sensor Name	CPU_TEMP_04	FAN_SPEED_01	FAN_SPEED_02	FAN_SPEED_03	FAN_SPEED_04	FAN_SPEED_05	FAN_SPEED_06
Sensor Type	0x01	0x04	0x04	0x04	0x04	0x04	0x04
Event Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Entity ID	0x03	0x1D	0x1D	0x1D	0x1D	0x1D	0x1D
Instance	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Initialization	0x7F	0x7F	0x7F	0x7F	0x7F	0x7F	0x7F
Capabilities	0x68	0x68	0x68	0x68	0x68	0x68	0x68
AE/LTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
AE/LTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DE/UTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
DE/UTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DR/ST/RT Mask	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636
DR/ST/RT (BIT)	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/
LNR	0x00	0x16	0x1A	0x16	0x1A	0x16	0x1A
LC	0x04	0x17	0x1B	0x17	0x1B	0x17	0x1B
LNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UC	0x61	0x83	0x99	0x83	0x99	0x83	0x99
UNR	0x66	0x85	0x9B	0x85	0x9B	0x85	0x9B
Resolution							

	22	23	24	25	26	27	28
Sensor Number	0x36	0x37	0x38	0x39	0x64	0x65	0x6C
Sensor Name	FAN_SPEED_07	FAN_SPEED_08	FAN_SPEED_09	FAN_SPEED_10	PSU_TEMP_01	PSU_TEMP_02	POWER_WATTS
Sensor Type	0x04	0x04	0x04	0x04	0x01	0x01	0x03
Event Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Entity ID	0x1D	0x1D	0x1D	0x1D	0x0A	0x0A	0x0A
Instance	0x00	0x00	0x00	0x00	0x04	0x05	0x00
Initialization	0x7F	0x7F	0x7F	0x7F	0x77	0x77	0x7F
Capabilities	0x68	0x68	0x68	0x68	0x48	0x48	0x68
AE/LTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x0000	0x0000	0x0000
AE/LTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/			
DE/UTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x0000	0x0000	0x0000
DE/UTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/			
DR/ST/RT Mask	0x3636	0x3636	0x3636	0x3636	0x0000	0x0000	0x0000
DR/ST/RT (BIT)	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/			
LNR	0x16	0x1A	0x16	0x1A	0x00	0x00	0x00
LC	0x17	0x1B	0x17	0x1B	0x00	0x00	0x01
LNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UNC	0x00	0x00	0x00	0x00	0x00	0x00	0xFF
UC	0x83	0x99	0x83	0x99	0x46	0x46	0xFF
UNR	0x85	0x9B	0x85	0x9B	0x4B	0x4B	0xFF
Resolution							

- AM/LTR : Assertion Event Mask / Lower Threshold Reading Mask
- DEM/UTR : De-assertion Event Mask / Upper Threshold Reading Mask
- DE/UTR: Discrete Reading Mask / Settable Threshold Mask, Readable Threshold Mask

- LNR : Lower non-recoverable Threshold
- LC : Lower critical Threshold
- LNC : Lower non-critical Threshold
- UNC : Upper non-critical Threshold
- UC : Upper critical Threshold
- UNR : Upper non-recoverable Threshold

	29	30	31	32	33	34	35
Sensor Number	0x2A	0x2B	0x2E	0x2F	0x51	0x52	0x54
Sensor Name	MEM_VOLTS_01	MEM_VOLTS_02	MEM_VOLTS_03	MEM_VOLTS_04	MEM_VOLTS_05	MEM_VOLTS_06	MEM_VOLTS_07
Sensor Type	0x02	0x02	0x02	0x02	0x02	0x02	0x02
Event Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Entity ID	0x07	0x07	0x07	0x07	0x07	0x07	0x07
Instance	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Initialization	0x7F	0x7F	0x7F	0x7F	0x7F	0x7F	0x7F
Capabilities	0x68	0x68	0x68	0x68	0x68	0x68	0x68
AE/LTR Mask	0x2204	0x2204	0x2204	0x2204	0x2204	0x2204	0x2204
AE/LTR (BIT)	2/9/13/	2/9/13/	2/9/13/	2/9/13/	2/9/13/	2/9/13/	2/9/13/
DE/UTR Mask	0x2204	0x2204	0x2204	0x2204	0x2204	0x2204	0x2204
DE/UTR (BIT)	2/9/13/	2/9/13/	2/9/13/	2/9/13/	2/9/13/	2/9/13/	2/9/13/
DR/ST/RT Mask	0x1212	0x1212	0x1212	0x1212	0x1212	0x1212	0x1212
DR/ST/RT (BIT)	1/4/9/12/	1/4/9/12/	1/4/9/12/	1/4/9/12/	1/4/9/12/	1/4/9/12/	1/4/9/12/
LNR	0x00	0x00	0x00	0x00	0x00	0x00	0x00
LC	0x97	0x97	0x97	0x97	0x97	0x97	0x97
LNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UNC	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
UC	0xF5	0xF5	0xF5	0xF5	0xF5	0xF5	0xF5
UNR	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
Resolution							

	36	37	38	39	40	41	42
Sensor Number	0x55	0x28	0x2C	0x50	0x53	0x21	0x22
Sensor Name	MEM_VOLTS_08	CPU_VOLTS_01	CPU_VOLTS_02	CPU_VOLTS_03	CPU_VOLTS_04	SYS_VOLTS_01	SYS_VOLTS_02
Sensor Type	0x02	0x02	0x02	0x02	0x02	0x02	0x02
Event Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Entity ID	0x07	0x07	0x07	0x07	0x07	0x07	0x07
Instance	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Initialization	0x7F	0x7F	0x7F	0x77	0x7F	0x7F	0x7F
Capabilities	0x68	0x68	0x68	0x68	0x68	0x68	0x68
AE/LTR Mask	0x2204	0x0325	0x0325	0x0325	0x0325	0x2204	0x2204
AE/LTR (BIT)	2/9/13/	0/2/5/8/9/	0/2/5/8/9/	0/2/5/8/9/	0/2/5/8/9/	2/9/13/	2/9/13/
DE/UTR Mask	0x2204	0x3285	0x3285	0x3285	0x3285	0x2204	0x2204
DE/UTR (BIT)	2/9/13/	0/2/7/9/12/13/	0/2/7/9/12/13/	0/2/7/9/12/13/	0/2/7/9/12/13/	2/9/13/	2/9/13/
DR/ST/RT Mask	0x1212	0x1B1B	0x1B1B	0x1B1B	0x1B1B	0x1212	0x1212
DR/ST/RT (BIT)	1/4/9/12/	0/1/3/4/8/9/11/12/	0/1/3/4/8/9/11/12/	0/1/3/4/8/9/11/12/	0/1/3/4/8/9/11/12/	1/4/9/12/	1/4/9/12/
LNR	0x00	0x00	0x00	0x00	0x00	0x00	0x00
LC	0x97	0x8E	0x8E	0x8E	0x8E	0xB6	0xDE
LNC	0x00	0x92	0x92	0x92	0x92	0x00	0x00
UNC	0xFF	0xD5	0xD5	0xD5	0xD5	0xFF	0xFF
UC	0xF5	0xDB	0xDB	0xDB	0xDB	0xC9	0xF5
UNR	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
Resolution							

- AM/LTR : Assertion Event Mask / Lower Threshold Reading Mask
- DEM/UTR : De-assertion Event Mask / Upper Threshold Reading Mask
- DE/UTR: Discrete Reading Mask / Settable Threshold Mask, Readable Threshold Mask

- LNR : Lower non-recoverable Threshold
- LC : Lower critical Threshold
- LNC : Lower non-critical Threshold
- UNC : Upper non-critical Threshold
- UC : Upper critical Threshold
- UNR : Upper non-recoverable Threshold

	43	44	45	46	47	48	49
Sensor Number	0x20	0x68	0x69	0x6A	0x6B	0x40	0x41
Sensor Name	SYS_VOLTS_03	INPUT_VOLTS_01	INPUT_VOLTS_02	OUTPUT_VOLTS_01	OUTPUT_VOLTS_02	CPU_STATUS_01	CPU_STATUS_02
Sensor Type	0x02	0x02	0x02	0x02	0x02	0x07	0x07
Event Type	0x01	0x01	0x01	0x01	0x01	0x6F	0x6F
Entity ID	0x07	0x0A	0x0A	0x0A	0x0A	0x03	0x03
Instance	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Initialization	0x7F	0x7F	0x7F	0x7F	0x7F	0x63	0x63
Capabilities	0x68	0x68	0x68	0x68	0x68	0x68	0x40
AE/LTR Mask	0x2204	0x0000	0x0000	0x0000	0x0000	0x0002	0x0002
AE/LTR (BIT)	2/9/13/					1/	1/
DE/UTR Mask	0x2204	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
DE/UTR (BIT)	2/9/13/						
DR/ST/RT Mask	0x1212	0x0000	0x0000	0x0000	0x0000	0x0082	0x0082
DR/ST/RT (BIT)	1/4/9/12/					1/7/	1/7/
LNR	0x00	0xA6	0xA6	0x00	0x00	0x00	0x00
LC	0xE2	0xA9	0xA9	0x00	0x00	0x00	0x00
LNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UNC	0xFF	0x00	0x00	0x00	0x00	0x00	0x00
UC	0xFA	0xC1	0xC1	0xFF	0xFF	0x00	0x00
UNR	0xFF	0xC4	0xC4	0xFF	0xFF	0x00	0x00
Resolution							

	50	51	52	53	54	55	56
Sensor Number	0x42	0x43	0x48	0x49	0x4A	0x4B	0x80
Sensor Name	CPU_STATUS_03	CPU_STATUS_04	CPU_VR_Temp_01	CPU_VR_Temp_02	CPU_VR_Temp_03	CPU_VR_Temp_04	MEM_TEMP_01_A0
Sensor Type	0x07	0x07	0x01	0x01	0x01	0x01	0x01
Event Type	0x6F	0x6F	0x01	0x01	0x01	0x01	0x01
Entity ID	0x03	0x03	0x07	0x07	0x07	0x07	0x08
Instance	0x00	0x00	0x03	0x04	0x05	0x06	0x00
Initialization	0x63	0x63	0x77	0x77	0x77	0x77	0x77
Capabilities	0x40	0x40	0x68	0x68	0x68	0x68	0x48
AE/LTR Mask	0x0002	0x0002	0x0280	0x0280	0x0280	0x0280	0x6A14
AE/LTR (BIT)	1/	1/	7/9/	7/9/	7/9/	7/9/	2/4/9/11/13/14/
DE/UTR Mask	0x0000	0x0000	0x3280	0x3280	0x3280	0x3280	0x6A14
DE/UTR (BIT)			7/9/12/13/	7/9/12/13/	7/9/12/13/	7/9/12/13/	2/4/9/11/13/14/
DR/ST/RT Mask	0x0082	0x0082	0x1818	0x1818	0x1818	0x1818	0x3636
DR/ST/RT (BIT)	1/7/	1/7/	3/4/11/12/	3/4/11/12/	3/4/11/12/	3/4/11/12/	1/2/4/5/9/10/12/13/
LNR	0x00	0x00	0x00	0x00	0x00	0x00	0x00
LC	0x00	0x00	0x00	0x00	0x00	0x00	0x04
LNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UNC	0x00	0x00	0x78	0x78	0x78	0x78	0x00
UC	0x00	0x00	0x7D	0x7D	0x7D	0x7D	0x52
UNR	0x00	0x00	0xFF	0xFF	0xFF	0xFF	0x55
Resolution							

- AM/LTR : Assertion Event Mask / Lower Threshold Reading Mask
- DEM/UTR : De-assertion Event Mask / Upper Threshold Reading Mask
- DE/UTR: Discrete Reading Mask / Settable Threshold Mask, Readable Threshold Mask

- LNR : Lower non-recoverable Threshold
- LC : Lower critical Threshold
- LNC : Lower non-critical Threshold
- UNC : Upper non-critical Threshold
- UC : Upper critical Threshold
- UNR : Upper non-recoverable Threshold

	57	58	59	60	61	62	63
Sensor Number	0x81	0x82	0x83	0x84	0x85	0x86	0x87
Sensor Name	MEM_TEMP_01_A1	MEM_TEMP_01_B0	MEM_TEMP_01_B1	MEM_TEMP_01_C0	MEM_TEMP_01_C1	MEM_TEMP_01_D0	MEM_TEMP_01_D1
Sensor Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Event Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Entity ID	0x08	0x08	0x08	0x08	0x08	0x08	0x08
Instance	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Initialization	0x77	0x77	0x77	0x77	0x77	0x77	0x77
Capabilities	0x48	0x48	0x48	0x48	0x48	0x48	0x48
AE/LTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
AE/LTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DE/UTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
DE/UTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DR/ST/RT Mask	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636
DR/ST/RT (BIT)	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/
LNR	0x00	0x00	0x00	0x00	0x00	0x00	0x00
LC	0x04	0x04	0x04	0x04	0x04	0x04	0x04
LNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UC	0x52	0x52	0x52	0x52	0x52	0x52	0x52
UNR	0x55	0x55	0x55	0x55	0x55	0x55	0x55
Resolution							

	64	65	66	67	68	69	70
Sensor Number	0x88	0x89	0x8A	0x8B	0x8C	0x8D	0x8E
Sensor Name	MEM_TEMP_01_E0	MEM_TEMP_01_E1	MEM_TEMP_01_F0	MEM_TEMP_01_F1	MEM_TEMP_02_A0	MEM_TEMP_02_A1	MEM_TEMP_02_B0
Sensor Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Event Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Entity ID	0x08	0x08	0x08	0x08	0x08	0x08	0x08
Instance	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Initialization	0x77	0x77	0x77	0x77	0x77	0x77	0x77
Capabilities	0x48	0x48	0x48	0x48	0x48	0x48	0x48
AE/LTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
AE/LTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DE/UTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
DE/UTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DR/ST/RT Mask	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636
DR/ST/RT (BIT)	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/
LNR	0x00	0x00	0x00	0x00	0x00	0x00	0x00
LC	0x04	0x04	0x04	0x04	0x04	0x04	0x04
LNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UC	0x52	0x52	0x52	0x52	0x52	0x52	0x52
UNR	0x55	0x55	0x55	0x55	0x55	0x55	0x55
Resolution							

- AM/LTR : Assertion Event Mask / Lower Threshold Reading Mask
- DEM/UTR : De-assertion Event Mask / Upper Threshold Reading Mask
- DE/UTR: Discrete Reading Mask / Settable Threshold Mask, Readable Threshold Mask

- LNR : Lower non-recoverable Threshold
- LC : Lower critical Threshold
- LNC : Lower non-critical Threshold
- UNC : Upper non-critical Threshold
- UC : Upper critical Threshold
- UNR : Upper non-recoverable Threshold

	71	72	73	74	75	76	77
Sensor Number	0x8F	0x90	0x91	0x92	0x93	0x94	0x95
Sensor Name	MEM_TEMP_02_B1	MEM_TEMP_02_C0	MEM_TEMP_02_C1	MEM_TEMP_02_D0	MEM_TEMP_02_D1	MEM_TEMP_02_E0	MEM_TEMP_02_E1
Sensor Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Event Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Entity ID	0x08	0x08	0x08	0x08	0x08	0x08	0x08
Instance	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Initialization	0x77	0x77	0x77	0x77	0x77	0x77	0x77
Capabilities	0x48	0x48	0x48	0x48	0x48	0x48	0x48
AE/LTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
AE/LTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DE/UTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
DE/UTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DR/ST/RT Mask	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636
DR/ST/RT (BIT)	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/
LNR	0x00	0x00	0x00	0x00	0x00	0x00	0x00
LC	0x04	0x04	0x04	0x04	0x04	0x04	0x04
LNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UC	0x52	0x52	0x52	0x52	0x52	0x52	0x52
UNR	0x55	0x55	0x55	0x55	0x55	0x55	0x55
Resolution							

	78	79	80	81	82	83	84
Sensor Number	0x96	0x97	0x98	0x99	0x9A	0x9B	0x9C
Sensor Name	MEM_TEMP_02_F0	MEM_TEMP_02_F1	MEM_TEMP_03_A0	MEM_TEMP_03_A1	MEM_TEMP_03_B0	MEM_TEMP_03_B1	MEM_TEMP_03_C0
Sensor Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Event Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Entity ID	0x08	0x08	0x08	0x08	0x08	0x08	0x08
Instance	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Initialization	0x77	0x77	0x77	0x77	0x77	0x77	0x77
Capabilities	0x48	0x48	0x48	0x48	0x48	0x48	0x48
AE/LTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
AE/LTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DE/UTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
DE/UTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DR/ST/RT Mask	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636
DR/ST/RT (BIT)	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/
LNR	0x00	0x00	0x00	0x00	0x00	0x00	0x00
LC	0x04	0x04	0x04	0x04	0x04	0x04	0x04
LNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UC	0x52	0x52	0x52	0x52	0x52	0x52	0x52
UNR	0x55	0x55	0x55	0x55	0x55	0x55	0x55
Resolution							

- AM/LTR : Assertion Event Mask / Lower Threshold Reading Mask
- DEM/UTR : De-assertion Event Mask / Upper Threshold Reading Mask
- DE/UTR: Discrete Reading Mask / Settable Threshold Mask, Readable Threshold Mask

- LNR : Lower non-recoverable Threshold
- LC : Lower critical Threshold
- LNC : Lower non-critical Threshold
- UNC : Upper non-critical Threshold
- UC : Upper critical Threshold
- UNR : Upper non-recoverable Threshold

	85	86	87	88	89	90	91
Sensor Number	0x9D	0x9E	0x9F	0xA0	0xA1	0xA2	0xA3
Sensor Name	MEM_TEMP_03_C1	MEM_TEMP_03_D0	MEM_TEMP_03_D1	MEM_TEMP_03_E0	MEM_TEMP_03_E1	MEM_TEMP_03_F0	MEM_TEMP_03_F1
Sensor Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Event Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Entity ID	0x08	0x08	0x08	0x08	0x08	0x08	0x08
Instance	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Initialization	0x77	0x77	0x77	0x77	0x77	0x77	0x77
Capabilities	0x48	0x48	0x48	0x48	0x48	0x48	0x48
AE/LTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
AE/LTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DE/UTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
DE/UTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DR/ST/RT Mask	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636
DR/ST/RT (BIT)	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/
LNR	0x00	0x00	0x00	0x00	0x00	0x00	0x00
LC	0x04	0x04	0x04	0x04	0x04	0x04	0x04
LNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UC	0x52	0x52	0x52	0x52	0x52	0x52	0x52
UNR	0x55	0x55	0x55	0x55	0x55	0x55	0x55
Resolution							

	92	93	94	95	96	97	98
Sensor Number	0xA4	0xA5	0xA7	0xA6	0xA8	0xA9	0xAA
Sensor Name	MEM_TEMP_04_A0	MEM_TEMP_04_A1	MEM_TEMP_04_B1	MEM_TEMP_04_B0	MEM_TEMP_04_C0	MEM_TEMP_04_C1	MEM_TEMP_04_D0
Sensor Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Event Type	0x01	0x01	0x01	0x01	0x01	0x01	0x01
Entity ID	0x08	0x08	0x08	0x08	0x08	0x08	0x08
Instance	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Initialization	0x77	0x77	0x77	0x77	0x77	0x77	0x77
Capabilities	0x48	0x48	0x48	0x48	0x48	0x48	0x48
AE/LTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
AE/LTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DE/UTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14
DE/UTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/
DR/ST/RT Mask	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636	0x3636
DR/ST/RT (BIT)	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/
LNR	0x00	0x00	0x00	0x00	0x00	0x00	0x00
LC	0x04	0x04	0x04	0x04	0x04	0x04	0x04
LNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UC	0x52	0x52	0x52	0x52	0x52	0x52	0x52
UNR	0x55	0x55	0x55	0x55	0x55	0x55	0x55
Resolution							

- AM/LTR : Assertion Event Mask / Lower Threshold Reading Mask
- DEM/UTR : De-assertion Event Mask / Upper Threshold Reading Mask
- DE/UTR: Discrete Reading Mask / Settable Threshold Mask, Readable Threshold Mask

- LNR : Lower non-recoverable Threshold
- LC : Lower critical Threshold
- LNC : Lower non-critical Threshold
- UNC : Upper non-critical Threshold
- UC : Upper critical Threshold
- UNR : Upper non-recoverable Threshold

	99	100	101	102	103	104	105
Sensor Number	0xAB	0xAC	0xAD	0xAE	0xAF	0x10	0x11
Sensor Name	MEM_TEMP_04_D1	MEM_TEMP_04_E0	MEM_TEMP_04_E1	MEM_TEMP_04_F0	MEM_TEMP_04_F1	HDD_STATUS_01	HDD_STATUS_02
Sensor Type	0x01	0x01	0x01	0x01	0x01	0x0D	0x0D
Event Type	0x01	0x01	0x01	0x01	0x01	0x6F	0x6F
Entity ID	0x08	0x08	0x08	0x08	0x08	0x04	0x04
Instance	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Initialization	0x77	0x77	0x77	0x77	0x77	0x7F	0x7F
Capabilities	0x48	0x48	0x48	0x48	0x48	0x60	0x60
AE/LTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x0003	0x0003
AE/LTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	0/1/	0/1/
DE/UTR Mask	0x6A14	0x6A14	0x6A14	0x6A14	0x6A14	0x0000	0x0000
DE/UTR (BIT)	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/	2/4/9/11/13/14/		
DR/ST/RT Mask	0x3636	0x3636	0x3636	0x3636	0x3636	0x0003	0x0003
DR/ST/RT (BIT)	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	1/2/4/5/9/10/12/13/	0/1/	0/1/
LNR	0x00	0x00	0x00	0x00	0x00	0x00	0x00
LC	0x04	0x04	0x04	0x04	0x04	0x00	0x00
LNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UNC	0x00	0x00	0x00	0x00	0x00	0x00	0x00
UC	0x52	0x52	0x52	0x52	0x52	0x00	0x00
UNR	0x55	0x55	0x55	0x55	0x55	0x00	0x00
Resolution							

	106	107	108	109	110	111	112
Sensor Number	0x12	0x13	0x14	0x15			
Sensor Name	HDD_STATUS_03	HDD_STATUS_04	HDD_STATUS_05	HDD_STATUS_06			
Sensor Type	0x0D	0x0D	0x0D	0x0D			
Event Type	0x6F	0x6F	0x6F	0x6F			
Entity ID	0x04	0x04	0x04	0x04			
Instance	0x00	0x00	0x00	0x00			
Initialization	0x7F	0x7F	0x7F	0x7F			
Capabilities	0x60	0x60	0x60	0x60			
AE/LTR Mask	0x008F	0x008F	0x008F	0x008F			
AE/LTR (BIT)	0/1/2/3/7/	0/1/2/3/7/	0/1/2/3/7/	0/1/2/3/7/			
DE/UTR Mask	0x0000	0x0000	0x0000	0x0000			
DE/UTR (BIT)							
DR/ST/RT Mask	0x008F	0x008F	0x008F	0x008F			
DR/ST/RT (BIT)	0/1/2/3/7/	0/1/2/3/7/	0/1/2/3/7/	0/1/2/3/7/			
LNR	0x00	0x00	0x00	0x00			
LC	0x00	0x00	0x00	0x00			
LNC	0x00	0x00	0x00	0x00			
UNC	0x00	0x00	0x00	0x00			
UC	0x00	0x00	0x00	0x00			
UNR	0x00	0x00	0x00	0x00			
Resolution							

- AM/LTR : Assertion Event Mask / Lower Threshold Reading Mask
- DEM/UTR : De-assertion Event Mask / Upper Threshold Reading Mask
- DE/UTR: Discrete Reading Mask / Settable Threshold Mask, Readable Threshold Mask

- LNR : Lower non-recoverable Threshold
- LC : Lower critical Threshold
- LNC : Lower non-critical Threshold
- UNC : Upper non-critical Threshold
- UC : Upper critical Threshold
- UNR : Upper non-recoverable Threshold

	1	2	3	4	5	6	7
Sensor Number	0x60	0x61	0xB0	0xB1	0xB2	0xB3	0xB4
Sensor Name	PSU_STATUS_01	PSU_STATUS_02	MEM_STATUS_01	MEM_STATUS_02	MEM_STATUS_03	MEM_STATUS_04	MEM_STATUS_05
Sensor Type	0x08	0x08	0x0C	0x0C	0x0C	0x0C	0x0C
Event Type	0x6F	0x6F	0x6F	0x6F	0x6F	0x6F	0x6F
Entity ID	0x0A	0x0A	0x20	0x20	0x20	0x20	0x20
Instance	0x00	0x01	0x00	0x00	0x00	0x00	0x00
Initialization	0x67	0x67	0x67	0x67	0x67	0x67	0x67
Capabilities	0x40	0x40	0x60	0x60	0x60	0x60	0x60
AE/LTR Mask	0x004B	0x004B	0x7FFF	0x7FFF	0x7FFF	0x7FFF	0x7FFF
AE/LTR (BIT)	0/1/3/6/	0/1/3/6/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/
DE/UTR Mask	0x004A	0x004A	0x7FFF	0x7FFF	0x0000	0x0000	0x0000
DE/UTR (BIT)	1/3/6/	1/3/6/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/			
DR/ST/RT Mask	0x004B	0x004B	0x7FFF	0x7FFF	0x7FFF	0x7FFF	0x7FFF
DR/ST/RT (BIT)	0/1/3/6/	0/1/3/6/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/
SRS/SD	0x0000	0x0000	0x8101	0x8101	0x8101	0x8101	0x8101
SRS/SD (BIT)			0/8/15/	0/8/15/	0/8/15/	0/8/15/	0/8/15/

	8	9	10	11	12	13	14
Sensor Number	0xB5	0xB6	0xB7	0xFE	0xFA	0xFD	0xF2
Sensor Name	MEM_STATUS_06	MEM_STATUS_07	MEM_STATUS_08	SEL	WATCHDOG2	PWR_UNIT_STATUS	PSU_REDUNANCY
Sensor Type	0x0C	0x0C	0x0C	0x10	0x23	0x09	0x08
Event Type	0x6F	0x6F	0x6F	0x6F	0x6F	0x6F	0x0B
Entity ID	0x20	0x20	0x20	0x06	0x00	0x0A	0x0A
Instance	0x00	0x00	0x00	0x02	0x09	0x00	0x09
Initialization	0x67	0x67	0x67	0xE7	0x7F	0x67	0x7F
Capabilities	0x60	0x60	0x60	0x40	0x68	0x40	0x68
AE/LTR Mask	0x7FFF	0x7FFF	0x7FFF	0x0034	0x010F	0x0000	0x0003
AE/LTR (BIT)	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	2/4/5/	0/1/2/3/8/		0/1/
DE/UTR Mask	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
DE/UTR (BIT)							
DR/ST/RT Mask	0x7FFF	0x7FFF	0x7FFF	0x0034	0x010F	0x0064	0x0003
DR/ST/RT (BIT)	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	0/1/2/3/4/5/6/7/8/9/10/ 11/12/13/14/	2/4/5/	0/1/2/3/8/	2/5/6/	0/1/
SRS/SD	0x8101	0x8101	0x8101	0x0000	0x8101	0x8101	0x8101
SRS/SD (BIT)	0/8/15/	0/8/15/	0/8/15/		0/8/15/	0/8/15/	0/8/15/

- AM/LTR : Assertion Event Mask / Lower Threshold Reading Mask
- DEM/UTR : De-assertion Event Mask / Upper Threshold Reading Mask
- DE/UTR: Discrete Reading Mask / Settable Threshold Mask, Readable Threshold Mask

- LNR : Lower non-recoverable Threshold
- LC : Lower critical Threshold
- LNC : Lower non-critical Threshold
- UNC : Upper non-critical Threshold
- UC : Upper critical Threshold
- UNR : Upper non-recoverable Threshold

	15	16	17	18	19	20	21
Sensor Number	0xB8	0xB9	0xBA	0xBB			
Sensor Name	CPU1_PROCHOT	CPU2_PROCHOT	CPU3_PROCHOT	CPU4_PROCHOT			
Sensor Type	0x01	0x01	0x01	0x01			
Event Type	0x03	0x03	0x03	0x03			
Entity ID	0x03	0x03	0x03	0x03			
Instance	0x00	0x00	0x00	0x00			
Initialization	0x67	0x67	0x67	0x67			
Capabilities	0x40	0x40	0x40	0x40			
AE/LTR Mask	0x0002	0x0002	0x0002	0x0002			
AE/LTR (BIT)	1/	1/	1/	1/			
DE/UTR Mask	0x0002	0x0002	0x0002	0x0002			
DE/UTR (BIT)	1/	1/	1/	1/			
DR/ST/RT Mask	0x0002	0x0002	0x0002	0x0002			
DR/ST/RT (BIT)	1/	1/	1/	1/			
SRS/SD	0x0100	0x0100	0x0100	0x0100			
SRS/SD (BIT)	8/	8/	8/	8/			

	1	2	3	4	5	6	7
Sensor Number	0xF4	0xF9	0xFC	0xF5			
Sensor Name	START_OF_POST	MngSysHealth	BUTTON	NMI			
Sensor Type	0x12	0x28	0x14	0x13			
Event Type	0x6F	0x6F	0x6F	0x6F			
Entity ID	0x22	0x2E	0x0C	0x2E			
Instance	0x00	0x00	0x00	0x00			
SRS/SD	0x0000	0x8101	0x0000	0x0000			
SRS/SD (BIT)		0/8/15/					

- AM/LTR : Assertion Event Mask / Lower Threshold Reading Mask
- DEM/UTR : De-assertion Event Mask / Upper Threshold Reading Mask
- DE/UTR: Discrete Reading Mask / Settable Threshold Mask, Readable Threshold Mask

- LNR : Lower non-recoverable Threshold
- LC : Lower critical Threshold
- LNC : Lower non-critical Threshold
- UNC : Upper non-critical Threshold
- UC : Upper critical Threshold
- UNR : Upper non-recoverable Threshold

11.2 Automatic CPU Thresholds (for Intel Platform only)

Items	Rule
CPU Maximum Temperature	CPU T-JMAX (It is according to CPU Specification)
Upper Non-Recoverable Temperature	CPU T-JMAX
Upper Critical Temperature	CPU T-JMAX - 1
Upper Non-Critical Temperature	CPU T-JMAX - 2

- CPU Thresholds of SDR (static) are default values. (please ignore CPU thresholds of SDR)
- The values are changed on Sensor(dynamic) rather than SDR(static) after system power on.

12. Supported Standard IPMI Commands

Key for Command Privilege Levels Table:

- b = command only generated by BMC, can be sent prior to a session being established
- b1 = command only generated by BMC, can only be delivered to a session-less channel, or a channel that has an active session
- b2 = command only generated by BMC, can be sent to a serial channel when serial port sharing is used and activating the SOL payload causes the serial session to be terminated.
- b3 = command only generated by BMC, can only be delivered to a session-less channel.
- p = works at any privilege level, can be sent prior to a session being established
- s = command executable via system interface only
- X = supported at given privilege level or higher
- I = command executable from local interfaces only (e.g. IPMB, SMBus, PCI Mgmt. bus or System Interface)
- C = Callback privilege
- U = User Privilege level
- = Operator Privilege level
- A = Administrator Privilege level
- App = Application Network Function Code
- S/E = Sensor/Event Network Function Code
- - = Reserved/unassigned, or OEM specified

12.1 IPMI Global Commands

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	Get Device ID	20.1	App(06h)	01h		X		
Yes	Broadcast 'Get Device ID'[1]	20.9	App(06h)	01h	I	I	I	I
Yes	Cold Reset	20.2	App(06h)	02h				X
Yes	Warm Reset	20.3	App(06h)	03h				X
Yes	Get Self Test Results	20.4	App(06h)	04h		X		
Yes	Manufacturing Test On	20.5	App(06h)	05h				X
Yes	Set ACPI Power State	20.6	App(06h)	06h				X
Yes	Get ACPI Power State	20.7	App(06h)	07h		X		
Yes	Get Device GUID	20.8	App(06h)	08h	X	X		
Yes	Get NetFn Support	21.2	App(06h)	09h		X		
Yes	Get Command Support	21.3	App(06h)	0Ah		X		
Yes	Get Command Sub-function Support	21.4	App(06h)	0Bh		X		
Yes	Get Configurable Commands	21.5	App(06h)	0Ch		X		
Yes	Get Configurable Command Sub-functions	21.6	App(06h)	0Dh		X		
Yes	Set Command Enables	21.7	App(06h)	60h				X
Yes	Get Command Enables	21.8	App(06h)	61h		X		
No	Set Command Sub-function Enables	21.9	App(06h)	62h				X
No	Get Command Sub-function Enables	21.10	App(06h)	63h		X		
Yes	Get OEM NetFn IANA Support	21.11	App(06h)	64h		X		

12.2 BMC Watchdog Timer Commands

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	Reset Watchdog Timer	27.5	App(06h)	22h			X	
Yes	Set Watchdog Timer	27.6	App(06h)	24h			X	
Yes	Get Watchdog Timer	27.7	App(06h)	25h		X		

12.3 BMC Device and Messaging Commands

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	Set BMC Global Enables	22.1	App(06h)	2Eh	S	S	S	S
Yes	Get BMC Global Enables	22.2	App(06h)	2Fh		X		
Yes	Clear Message Flags	22.3	App(06h)	30h	S	S	S	S
Yes	Get Message Flags	22.4	App(06h)	31h	S	S	S	S
Yes	Enable Message Channel Receive	22.5	App(06h)	32h	S	S	S	S
Yes	Get Message	22.6	App(06h)	33h	S	S	S	S
Yes	Send Message	22.7	App(06h)	34h		X[2]	X	
Yes	Read Event Message Buffer	22.8	App(06h)	35h	S	S	S	S
Yes	Get BT Interface Capabilities	22.10	App(06h)	36h		X		
Yes	Get System GUID	22.14	App(06h)	37h	P[3]	P[3]	P[3]	P[3]
Yes	Set System Info Parameters	22.14a	App(06h)	58h				X
Yes	Get System Info Parameters	22.14b	App(06h)	59h		X		

Yes	Get Channel Authentication Capabilities	22.13	App(06h)	38h	P[3]	P[3]	P[3]	P[3]
Yes	Get Session Challenge	22.15	App(06h)	39h	P[3]	P[3]	P[3]	P[3]
Yes	Activate Session	22.17	App(06h)	3Ah	P[3]	P[3]	P[3]	P[3]
Yes	Set Session Privilege Level	22.18	App(06h)	3Bh		X[4]		
Yes	Close Session	22.19	App(06h)	3Ch	X[5]			
Yes	Get Session Info	22.20	App(06h)	3Dh		X		
Yes	Get AuthCode	22.21	App(06h)	3Fh			X	
Yes	Set Channel Access	22.22	App(06h)	40h				X
Yes	Get Channel Access	22.23	App(06h)	41h		X		
Yes	Get Channel Info Command	22.24	App(06h)	42h		X		
Yes	Set User Access Command	22.26	App(06h)	43h				X
Yes	Get User Access Command	22.27	App(06h)	44h			X	
Yes	Set User Name	22.28	App(06h)	45h				X
Yes	Get User Name Command	22.29	App(06h)	46h			X	
Yes	Set User Password Command	22.30	App(06h)	47h				X
Yes	Activate Payload	24.1	App(06h)	48h		[10]	[10]	[10]
Yes	Deactivate Payload	24.1	App(06h)	48h		[10]	[10]	[10]
Yes	Get Payload Activation Status	24.2	App(06h)	49h		X		
Yes	Get Payload Instance Info	24.4	App(06h)	4Ah		X		
Yes	Set User Payload Access	24.5	App(06h)	4Bh				X
Yes	Get User Payload Access	24.6	App(06h)	4Ch			X	
Yes	Get Channel Payload Support	24.7	App(06h)	4Dh		X		
Yes	Get Channel Payload Version	24.8	App(06h)	4Eh		X		
Yes	Get Channel OEM Payload Info	24.9	App(06h)	4Fh		X		
Yes	Master Write-Read	22.11	App(06h)	52h			X	
Yes	Get Channel Cipher Suites	22.15	App(06h)	53h	P	P	P	P
Yes	Suspend/Resume Payload Encryption	24.3	App(06h)	54h		X[9]		
Yes	Set Channel Security Keys	22.25	App(06h)	55h				X
Yes	Get System Interface Capabilities	22.9	App(06h)	56h		X		

12.4 Chassis Device Commands

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	Get Chassis Capabilities	28.1	Chassis(00h)	00h		X		
Yes	Get Chassis Status	28.2	Chassis(00h)	01h		X		
Yes	Chassis Control	28.3	Chassis(00h)	02h			X	
No	Chassis Reset	28.4	Chassis(00h)	03h			X	
Yes	Chassis Identify	28.5	Chassis(00h)	04h			X	
Yes	Set Front Panel Button Enables	28.6	Chassis(00h)	0Ah				X
Yes	Set Chassis Capabilities	28.7	Chassis(00h)	05h				X
Yes	Set Power Restore Policy	28.8	Chassis(00h)	06h			X	
Yes	Set Power Cycle Interval	28.9	Chassis(00h)	0Bh				X
Yes	Get System Restart Cause	28.11	Chassis(00h)	07h		X		
Yes	Set System Boot Options	28.12	Chassis(00h)	08h			X[6]	
Yes	Get System Boot Options	28.13	Chassis(00h)	09h			X	
Yes	Get POH Counter	28.14	Chassis(00h)	0Fh		X		

12.5 Event Commands

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	Set Event Receiver	29.1	S/E(04h)	00h				X
Yes	Get Event Receiver	29.2	S/E(04h)	01h		X		
Yes	Platform Event (a.k.a. “Event Message”)	29.3	S/E(04h)	02h			X	

12.6 PEF and Alerting Commands

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	Get PEF Capabilities	30.1	S/E(04h)	10h		X		
Yes	Arm PEF Postpone Timer	30.2	S/E(04h)	11h				X
Yes	Set PEF Configuration Parameters	30.3	S/E(04h)	12h				X
Yes	Get PEF Configuration Parameters	30.4	S/E(04h)	13h			X	
Yes	Set Last Processed Event ID	30.5	S/E(04h)	14h				X
Yes	Get Last Processed Event ID	30.6	S/E(04h)	15h				X
Yes	Alert Immediate	30.7	S/E(04h)	16h				X
Yes	PET Acknowledge	30.8	S/E(04h)	17h	P	P	P	P

12.7 Sensor Device Commands

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	Get Device SDR Info	35.2	S/E(04h)	20h	I	I	I	I
Yes	Get Device SDR	35.3	S/E(04h)	21h	I	I	I	I
Yes	Reserve Device SDR Repository	35.4	S/E(04h)	22h	I	I	I	I
Yes	Get Sensor Reading Factors	35.5	S/E(04h)	23h		X		
Yes	Set Sensor Hysteresis	35.6	S/E(04h)	24h			X	
Yes	Get Sensor Hysteresis	35.7	S/E(04h)	25h		X		
Yes	Set Sensor Threshold	35.8	S/E(04h)	26h			X	
Yes	Get Sensor Threshold	35.9	S/E(04h)	27h		X		
Yes	Set Sensor Event Enable	35.10	S/E(04h)	28h			X	
Yes	Get Sensor Event Enable	35.11	S/E(04h)	29h		X		
Yes	Re-arm Sensor Events	35.12	S/E(04h)	2Ah			X	
Yes	Get Sensor Event Status	35.13	S/E(04h)	2Bh		X		
Yes	Get Sensor Reading	35.14	S/E(04h)	2Dh		X		
Yes	Set Sensor Type	35.15	S/E(04h)	2Eh			X	
Yes	Get Sensor Type	35.16	S/E(04h)	2Fh		X		
Yes	Set Sensor Reading And Event Status	35.17	S/E(04h)	30h			X	

12.8 FRU Device Commands

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	Get FRU Inventory Area Info	34.1	Storage(0Ah)	10h		X		
Yes	Read FRU Data	34.2	Storage(0Ah)	11h		X		
Yes	Write FRU Data	34.3	Storage(0Ah)	12h			X	

12.9 SDR Device Commands

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	Get SDR Repository Info	33.9	Storage(0Ah)	20h		X		
Yes	Get SDR Repository Allocation Info	33.10	Storage(0Ah)	21h		X		
Yes	Reserve SDR Repository	33.11	Storage(0Ah)	22h		X		
Yes	Get SDR	33.12	Storage(0Ah)	23h		X		
Yes	Add SDR	33.13	Storage(0Ah)	24h			X	
Yes	Partial Add SDR	33.14	Storage(0Ah)	25h			X	
No	Delete SDR	33.15	Storage(0Ah)	26h			X	
Yes	Clear SDR Repository	33.16	Storage(0Ah)	27h			X	
Yes	Get SDR Repository Time	33.17	Storage(0Ah)	28h		X		
No	Set SDR Repository Time	33.18	Storage(0Ah)	29h			X	
No	Enter SDR Repository Update Mode	33.19	Storage(0Ah)	2Ah			X	
No	Exit SDR Repository Update Mode	33.20	Storage(0Ah)	2Bh			X	
Yes	Run Initialization Agent	33.21	Storage(0Ah)	2Ch			X	

12.10 SEL Device Commands

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	Get SEL Info	31.2	Storage(0Ah)	40h		X		
Yes	Get SEL Allocation Info	31.3	Storage(0Ah)	41h		X		
Yes	Reserve SEL	31.4	Storage(0Ah)	42h		X		
Yes	Get SEL Entry	31.5	Storage(0Ah)	43h		X		
Yes	Add SEL Entry	31.6	Storage(0Ah)	44h			X	
Yes	Partial Add SEL Entry	31.7	Storage(0Ah)	45h			X	
Yes	Delete SEL Entry	31.8	Storage(0Ah)	46h			X	
Yes	Clear SEL	31.9	Storage(0Ah)	47h			X	
Yes	Get SEL Time	31.10	Storage(0Ah)	48h		X		
Yes	Set SEL Time	31.11	Storage(0Ah)	49h			X	
No	Get Auxiliary Log Status	31.12	Storage(0Ah)	5Ah		X		
No	Set Auxiliary Log Status	31.13	Storage(0Ah)	5Bh				X
Yes	Get SEL Time UTC Offset	31.11a	Storage(0Ah)	5Ch		X		
Yes	Set SEL Time UTC Offset	31.11b	Storage(0Ah)	5Dh			X	

12.11 LAN Device Commands

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	Set LAN Configuration Parameters	23.1	Transport(0Ch)	01h				X
Yes	Get LAN Configuration Parameters	23.2	Transport(0Ch)	02h			X	
Yes	Suspend BMC ARPs	23.3	Transport 0Ch)	03h				X
Yes	Get IP/UDP/RMCP Statistics	23.4	Transport(0Ch)	04h		X		

12.12 Serial/Modem Device Commands

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	Set Serial/Modem Configuration	25.1	Transport(0Ch)	10h				X
Yes	Get Serial/Modem Configuration	25.2	Transport(0Ch)	11h			X	
Yes	Set Serial/Modem Mux	25.3	Transport 0Ch)	12h			X	
Yes	Get TAP Response Codes	25.4	Transport(0Ch)	13h		X		
No	Set PPP UDP Proxy Transmit Data	25.5	Transport(0Ch)	14h	S	S	S	S
No	Get PPP UDP Proxy Transmit Data	25.6	Transport(0Ch)	15h	S	S	S	S
No	Send PPP UDP Proxy Packet	25.7	Transport 0Ch)	16h	S	S	S	S
No	Get PPP UDP Proxy Receive Data	25.8	Transport(0Ch)	17h	S	S	S	S
No	Serial/Modem Connection Active	25.9	Transport(0Ch)	18h	b	b	b	b
No	Callback	25.10	Transport(0Ch)	19h		[7]		X7
No	Set User Callback Options	25.11	Transport 0Ch)	1Ah				X
No	Get User Callback Options	25.12	Transport(0Ch)	1Bh		X		
No	Set Serial Routing Mux	25.13	Transport(0Ch)	1Ch				X
No	SOL Activating	26.1	Transport(0Ch)	20h	b2	b2	b2	b2
Yes	Set SOL Configuration Parameters	26.2	Transport 0Ch)	21h				X
Yes	Get SOL Configuration Parameters	26.3	Transport(0Ch)	22h		X		

12.13 Command Forwarding Commands

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
No	Forwarded Command	35b.4	Transport(0Ch)	30h	b3	b3	b3	b3
No	Set Forwarded Commands	35b.1	Transport(0Ch)	31h				X
No	Get Forwarded Commands	35b.2	Transport 0Ch)	32h		X		
No	Enable Forwarded Commands	35b.3	Transport(0Ch)	33h				X

12.14 Bridge Management Commands (ICMB)

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	Get Bridge State	[ICMB]	Bridge(02h)	00h		X		
Yes	Set Bridge State	[ICMB]	Bridge(02h)	01h			X	
Yes	Get ICMB Address	[ICMB]	Bridge(02h)	02h		X		
Yes	Set ICMB Address	[ICMB]	Bridge(02h)	03h			X	
Yes	Set Bridge ProxyAddress	[ICMB]	Bridge(02h)	04h			X	
Yes	Get Bridge Statistics	[ICMB]	Bridge(02h)	05h		X		
Yes	Get ICMB Capabilities	[ICMB]	Bridge(02h)	06h		X		
Yes	Clear Bridge Statistics	[ICMB]	Bridge(02h)	08h			X	
Yes	Get Bridge Proxy Address	[ICMB]	Bridge(02h)	09h		X		

Yes	Get ICMB Connector Info	[ICMB]	Bridge(02h)	0Ah		X		
No	Get ICMB Connection ID	[ICMB]	Bridge(02h)	0Bh		X		
No	Send ICMB Connection ID	[ICMB]	Bridge(02h)	0Ch		X		

12.15 Discovery Commands (ICMB)

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	PrepareForDiscovery	[ICMB]	Bridge(02h)	10h			X	
Yes	GetAddresses	[ICMB]	Bridge(02h)	11h		X		
Yes	SetDiscovered	[ICMB]	Bridge(02h)	12h			X	
Yes	GetChassisDeviceId	[ICMB]	Bridge(02h)	13h		X		
Yes	SetChassisDeviceId	[ICMB]	Bridge(02h)	14h			X	

12.16 Bridging Commands (ICMB)[8]

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	BridgeRequest	[ICMB]	Bridge(02h)	20h			X	
Yes	BridgeMessage	[ICMB]	Bridge(02h)	21h			X	

12.17 Event Commands (ICMB) [8]

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
Yes	GetEventCount	[ICMB]	Bridge(02h)	30h		X		
Yes	SetEventDestination	[ICMB]	Bridge(02h)	31h			X	
Yes	SetEventReceptionState	[ICMB]	Bridge(02h)	32h			X	
Yes	SendICMBEventMessage	[ICMB]	Bridge(02h)	33h			X	
Yes	GetEventDestination (optional)	[ICMB]	Bridge(02h)	34h		X		
Yes	GetEventReceptionState (optional)	[ICMB]	Bridge(02h)	35h		X		

12.18 OEM Commands for Bridge NetFn

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
No	OEM Commands	[ICMB]	Bridge(02h)	C0h-FEh	-	-	-	-

12.19 Other Bridge Commands

Support	Command	IPMI Spec Ref.	NetFn	CMD	C	U	O	A
No	Error Report (optional)	[ICMB]	Bridge(02h)	FFh		X		

1. This command is sent using the Broadcast format on IPMB. See command description for details.

2. A User can use a Send Message command to deliver a message to system software, but Operator privilege is required to use it to access other channels.

3. Command only applies to authenticated channels.

4. This is effectively a no-op if the user has a maximum privilege limit of User since the command could not be used to change the operating privilege level to a higher value.

5. A session operating at Callback, User, or Operator can only use this command to terminate their own session. An Administrator or system software can use the command to terminate any session.

6. There is a bit in this command that can only be set at Administrator privilege level.

7. Command available for all levels except for User level

8. See [ICMB] specification for command specifications.

9. The Suspend/Resume Payload Encryption command may be overridden by a configuration option for the particular payload type that forces encryption to be used. In this case, an Admin level command would typically be required to change the configuration.

10. The configuration parameters for a given

13. BMC Booting

The BMC provide the robust mechanism to make sure the correct firmware to be loaded.

13.1. Redundant Firmware Image

Redundant firmware only be supported in SD Card mode. If there is no SD card or SD function is disabled, BMC redundant firmware is disabled. Sometimes BMC boot fail from primary ROM(SPI), UBOOT of SPI is able to change booting device. Please refer to SD Storage Specification if you want to get more information.

13.2. Firmware Integrity Check

The BMC boot loader will verify the checksum of the loaded firmware image before executing it. If the boot loader detects that the loaded firmware image is invalid, it will not be executed. BMC will select another SD storage for boot. If Both of ROMs part are fail, BMC SOC will reboot by WDT again.

13.3. Boot Time

From the point of reset, the BMC boot to fully operational state and be responsive to the host on KCS channel within 30 seconds. And LAN channel interface will be enable after 78 seconds.

13.4. Boot Process

a. The SoC is going to fetch UBOOT code after AC on. If UBOOT of primary ROM fail during UBOOT stage, BMC firmware will not operate in operation mode because redundant firmware is not invoked. BMC always retry boot in primary of SPI ROM.

b. After boot successfully in UBOOT of SPI, UBOOT would check BMC image integrity. In normally, BMC boot from primary SPI. If boot over 300 seconds, BMC internal watchdog is expired. So it causes BMC reboot. In this moment, UBOOT will try to boot from SD storage (if supports).